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メタデータ	言語: eng 出版者: 公開日: 2020-08-26 キーワード (Ja): キーワード (En): 作成者: Yoshida, Koki, Konishi, Keiji, Hara, Naoyuki メールアドレス: 所属:
URL	http://hdl.handle.net/10466/00017019

Noname manuscript No.
(will be inserted by the editor)

Experimental observation of destabilization in a DC bus system and its stabilization with delayed feedback control

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Received: date / Accepted: date

Abstract Direct-current (DC) bus systems are expected to play a significant role in next-generation power technology because of the rapid development of power electronics. However, it is well known that the bus line voltage can become unstable when electric power through the bus line is constantly consumed by loads. Bifurcation analysis of this instability has been previously performed. It has been reported that in theory, delayed feedback control, which was developed to stabilize chaotic systems, can suppress this instability. For practical applications, it is necessary to confirm these analytical results with circuit experiments. In this study, the dynamics of a DC bus system without control and with delayed feedback control are experimentally investigated. The following three main results are obtained. First, bifurcation phenomena are experimentally found to occur with an increase in power consumption in the DC bus system without control. Second, it is experimentally found that delayed feedback control stabilizes the operating point. These results provide experimental evidence that delayed feedback control can be utilized as a stabilization method for DC bus systems. Third, it is experimentally demonstrated that the delayed feedback controller can track the operating point when the power consumption changes slowly, but not when it changes rapidly. A frequency-domain analysis is conducted to analytically estimate the upper limit of the acceptable power consumption rate of change. The estimated upper limit is useful for designing the controller and restricting the change rate of power consumption.

Keywords Direct-current bus system · Bifurcation · Delayed feedback control · Tracking

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1 Introduction

It has been established that nonlinear dynamics play an important role in alternating-current (AC) power-grid networks [1–5]. Recently, the rapid development of power electronics has accelerated the use of direct-current (DC) power equipment, such as computers, photovoltaic power generators, fuel cells, and storage batteries. DC bus systems are thus expected to play a significant role in next-generation power technology [6–10]. However, it is well known that the bus line voltage can become unstable and show oscillatory behavior when the electric power through the bus line is constantly consumed by loads [11,12]. Such power loads are called constant power loads (CPLs). The instability induced by CPLs is a crucial drawback for DC bus systems; thus, a considerable number of studies in the field of power electronics (for reviews, see [13–16]) have focused on the suppression of this type of instability.

The approaches based on impedance-based stability analysis [17,18], which reshape the impedance of a voltage source and a load, are commonly used for suppressing the operating point instabilities. The approaches, which utilize linearized dynamics at the operating point, can be achieved using either passive damping techniques [12,19,20] and active damping techniques [21–24]. In contrast, nonlinear control strategies, such as feedback linearization techniques [25–27] and sliding mode control [28–30], deal with the nonlinear properties around the operating point. The DC bus systems

that consist of multiple power sources and loads have recently been studied [31–34].

In the field of controlling chaos, adaptive control techniques, such as derivative control [35,36] and low- / high-pass first-order RC filter techniques [37–42], have been proposed and applied for the stabilization of unstable equilibrium points in nonlinear dynamical systems. Delayed feedback control, proposed by Pyragas [43], is a popular scheme for the stabilization of unstable periodic orbits or unstable equilibrium points in nonlinear dynamical systems[1] [38,44–46]. The adaptive control techniques and delayed feedback control have the following advantages. First, the control signal becomes zero during stabilization. Additionally, the locations of unstable operating points are not needed in the control law, which is thus simple and easily implemented. Finally, a stabilized operating point with a small control signal can be maintained even when a system parameter slowly changes.

In a previous study, we analytically investigated the dynamics of a DC bus system using bifurcation theory and utilized delayed feedback control [47]. Moreover, we extended our results to DC bus networks that include multiple power sources and loads [48]. However, we note two problems with our analytical study [47] when considering practical operation of the system. First, the analytical results have not been experimentally confirmed with real electronic circuits, where noise and parameter mismatch are not negligible. Second, even though the power consumption of a practical load changes with time due to changes in user demands, the robustness of the system against such changes has not been clarified.

The present study tackles the above two problems. First, the dynamics of a DC bus system without control and with delayed feedback control are experimentally confirmed with real electronic circuits. Bifurcation scenarios are experimentally found to occur when the power consumption is increased in the DC bus system without control. Furthermore, the results of the stability analysis of operating points in the DC bus system with control are found to agree well with the experimental results. Second, the present study experimentally demonstrates that the delayed feedback controller can track the operating point when the power consumption changes slowly, but cannot do so when it changes rapidly. We conduct a frequency-domain analysis to analytically estimate the upper limit of the acceptable power consumption rate of change. Furthermore, the estimated upper limit is confirmed by circuit experiments. The present study is a substantially extended version of our conference paper [49].

[1] In Appendix A, delayed feedback control is compared to the adaptive techniques.

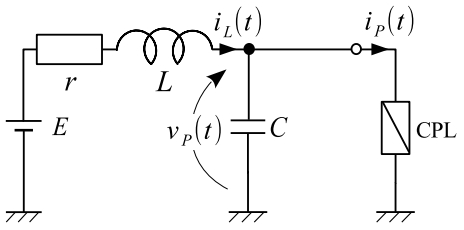


Fig. 1 DC bus system without control

2 DC bus system without control

This section reviews a mathematical model of a typical simple DC bus system without control [47]. The bus system is implemented using real electronic devices. The analytically obtained bifurcation curves and stability regions are experimentally confirmed.

2.1 Mathematical model [47]

Let us consider a typical simple DC bus system [12,16, 31,50] without control. This system consists of one DC voltage source and one CPL. The voltage source and the CPL have output and input filters, respectively, which contain resistors, inductors, and capacitors, for smoothing voltage. These filters are represented by equivalent resistance r, inductance L, and capacitance C, as shown in Fig. 1. E is the voltage of the source. $i_{\mathrm{L}}(t)$ is the line current. The DC bus voltage is denoted $v_{\mathrm{P}}(t)$. The CPL consumes constant power P regardless of $v_{\mathrm{P}}(t)$: $v_{\mathrm{P}}(t)i_{\mathrm{P}}(t) = P,\ \forall t \geq 0$. The bus system can be described as a dimensionless nonlinear dynamical system of the following form:

$$\begin{cases} \dot{x} = -\dfrac{a}{x} + by \\ \dot{y} = -x - by + 1 \end{cases} \tag{1}$$

via the following transformations,

$$x := \frac{1}{E} v_{\mathrm{P}},\ y := \frac{L}{rCE} i_{\mathrm{L}},\ \tau := \frac{t}{rC}, \tag{2}$$

$$a := \frac{rP}{E^2},\ b := \frac{r^2}{L/C}, \tag{3}$$

where $\dot{x}$ and $\dot{y}$ are the derivatives of the state variables x and y, respectively, with respect to dimensionless time τ.

The analytical results reported in our previous study [47] are summarized below. The dynamical system (1) has the following two equilibrium points:

$$\boldsymbol{p}_+ := [x_+^*, y_+^*]^T,\ \boldsymbol{p}_- := [x_-^*, y_-^*]^T, \tag{4}$$

$$x_\pm^* := \frac{1}{2}\left(1 \pm \sqrt{1-4a}\right),\ y_\pm^* := \frac{a}{bx_\pm^*}, \tag{5}$$

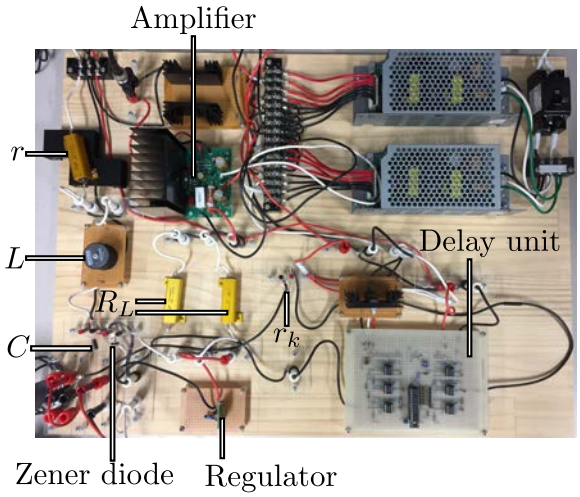


Fig. 2 Photograph of experimental setup

where $\boldsymbol{p}_+$ is the operating point of the DC bus system. For $a = rP/E^2 = 0$, the point $\boldsymbol{p}_+$ is a stable focus. The following bifurcation scenarios are derived with increasing $a > 0$. If $b < 1$ ($\Leftrightarrow r < \sqrt{L/C}$) holds, the following scenario occurs:

(a-1) An unstable limit cycle appears via a homoclinic bifurcation;

(a-2) The stable focus becomes an unstable focus via a Hopf bifurcation at

$$a = b/\left(1+b\right)^2; \tag{6}$$

(a-3) The unstable focus becomes an unstable node and then vanishes via a saddle-node bifurcation at

$$a = 1/4. \tag{7}$$

If $b > 1$ ($\Leftrightarrow r > \sqrt{L/C}$) holds, the following scenario occurs:

(b-1) The stable focus becomes a stable node and then vanishes via a saddle-node bifurcation at Eq. (7).

These bifurcation scenarios reported in [47] are experimentally confirmed in the following subsection.

2.2 Experimental results

This subsection describes the implementation of the DC bus system shown in Fig. 1 and the experimental confirmation of the analytical results.

2.2.1 Circuit implementation

The implemented DC bus system is shown in Fig. 2. Throughout this study, the passive device parameters are fixed at $E = 18.0\,\mathrm{V}$, $r = 21.9\,\Omega$, and $L = 22.7\,\mathrm{mH}$.

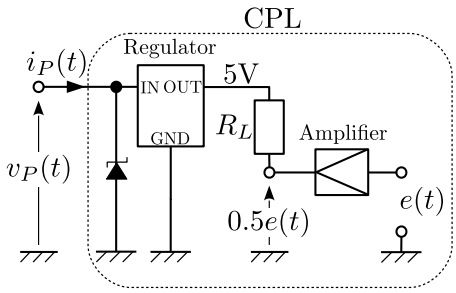


Fig. 3 CPL circuit

Note that r includes the resistance of the inductor. C and P are varied to confirm the analytically derived scenarios.

The CPL, implemented as illustrated in Fig. 3, consists of a switching regulator,[2] a Zener diode (1N5357BRLG, ON Semiconductor),[3] load resistance $R_L = 6\,\Omega$, an amplifier, and voltage source $e(t)$. The regulator operates such that an output voltage of 5 V is maintained regardless of the input voltage $v_\mathrm{p}(t)$. The amplifier acts as a voltage buffer (see Appendix B for details). Thus, the CPL consumes

$$P(t) = v_P(t) i_P(t) = \frac{5}{\eta R_L}\left\{5 - 0.5e(t)\right\} \tag{8}$$

for $e(t) < 10\,\mathrm{V}$, where $\eta = 0.9$ is the power conversion efficiency of the regulator. Equation (8) indicates that the consumed power $P(t)$ can be easily changed by adjusting the voltage source $e(t)$.

2.2.2 Confirmation of analytical results

This subsection describes the experimental confirmation of events **(a-1)**–**(a-3)** and **(b-1)** in the analytically derived scenarios.

(a-1) The circuit parameters are set to $C = 15.4\,\mu\mathrm{F}$ ($\Leftrightarrow b = 0.33$) and $P = 2.7\,\mathrm{W}$ ($\Leftrightarrow a = 0.18$). The trajectories from the two closed initial points $\big(x(0), y(0)\big) = (0.60, 1.18)$ and $(0.59, 1.23)$ are shown in Fig. 4. The gray trajectory, from the first point, spirals toward the equilibrium point $\boldsymbol{p}_+$, and the black trajectory, from the second point, spirals out. These trajectories imply that there exists an unstable limit cycle passing between these two initial points.

[2] We replace the capacitor for filtering, which had been implemented in a regulator (LM2675-5.0EVAL, Texas Instruments), by five 1 µF capacitors and one 0.1 µF capacitor. They are included in C.

[3] A diode with a Zener voltage of 20 V is used in the bus line to avoid high voltages being applied to devices connected to the bus line.

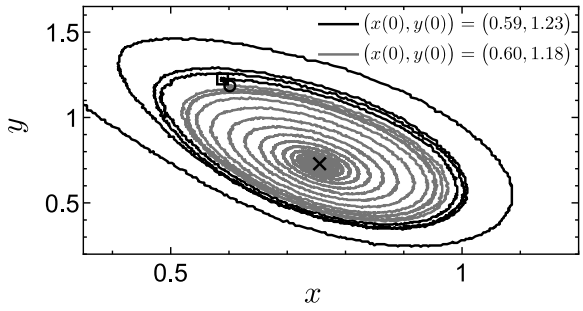


Fig. 4 Trajectories from initial points $\big(x(0), y(0)\big) = (0.60, 1.18)$ (◯) and $(0.59, 1.23)$ (□) without control (gray and black lines, respectively). Symbol × denotes equilibrium point $\boldsymbol{p}_+$

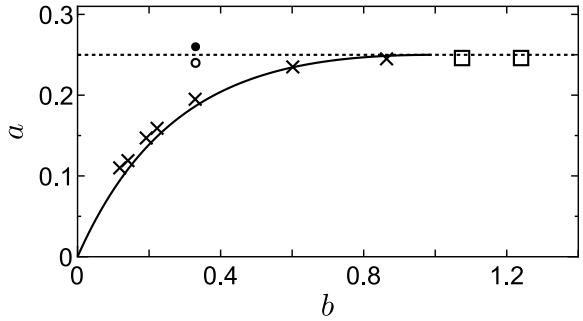


Fig. 5 Confirmation of bifurcation curves of Hopf (6) (solid line) and saddle-node (7) (dotted lines) bifurcations. With C ($\Leftrightarrow b$) held constant at various values, $v_P(t)$ spirals toward infinity and diverges without spiraling when P ($\Leftrightarrow a$) is increased above the values corresponding to the points labeled × and □, respectively. Points in the upper left side of the plot labeled with open and closed circles correspond to conditions in Figs. 6(a) and 6(b), respectively

(a-2), (b-1) As illustrated in Fig. 5, the Hopf (6) and saddle-node (7) bifurcation curves are confirmed by repeating the following procedure for various values of C ($\Leftrightarrow b$).

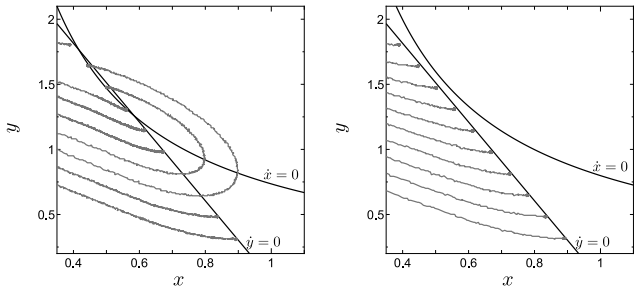
Step 1 A new value for C ($\Leftrightarrow b$) is selected, and P is set to 0 ($\Leftrightarrow a = 0$).

Step 2 P ($\Leftrightarrow a$) is gradually increased until $v_P(t)$ becomes unstable.

Step 3 The value of P ($\Leftrightarrow a$) just before $v_P(t)$ becomes unstable is obtained.

The symbols × and □ plotted on the Hopf (6) and saddle-node (7) bifurcation curves in Fig. 5 represent the values obtained in Step 3. The voltage $v_P(t)$ is found to spiral toward infinity and diverge without spiraling when P ($\Leftrightarrow a$) is increased above the points labeled × and □, respectively. This plot indicates that the experimental bifurcation results are in good agreement with the analytical results.

(a-3) It is then experimentally confirmed that the equilibrium points disappear through the saddle-node bifurcation. The power is set to $P = 3.6\,\mathrm{W}$ ($\Leftrightarrow a = 0.24$) and $P = 3.9\,\mathrm{W}$ ($\Leftrightarrow a = 0.26$), which, respectively, correspond to the open and closed circles in Fig. 5. Figures 6(a) and 6(b) show the analytical nullclines $\dot{x} = 0$ and $\dot{y} = 0$ for the open and closed circles, respectively. The initial points of the circuit are set on the nullcline $\dot{y} = 0$. Appendix C shows the procedure used for setting the initial points in the experiments. For the case with the lower power (Fig. 6(a)), the trajectories from two of the initial points move rightward from the nullcline, with those from the others moving leftward. The behavior of these trajectories suggests that two equilibrium points exist on the nullcline. In contrast, for the case with the higher power (Fig. 6(b)), all of the trajectories move leftward from the nullcline, implying that there is no equilibrium point on the nullcline. These results suggest that the equilibrium points disappear through the saddle-node bifurcation.



(a) $a = 0.24$ (b) $a = 0.26$

Fig. 6 Analytical nullclines $\dot{x} = 0$ and $\dot{y} = 0$ (black lines) and experimental trajectories (gray lines) from nullcline $\dot{y} = 0$ for (a) $a = 0.24$ and (b) $a = 0.26$ corresponding to open and closed circles in Fig. 5, respectively

3 DC bus system with control

This section reviews a previously reported mathematical model of a DC bus system with control and its stability analysis [47]. A delayed feedback controller is implemented using real electronic devices and applied to the DC bus line. The stabilization and tracking performance is confirmed experimentally.

3.1 Mathematical model [47,48]

This subsection briefly reviews the previously reported derivation and stability analysis of the mathematical model of a DC bus system with control [47]. As shown in Fig. 7, in this model, a delayed feedback controller is added to the bus line. This controller injects the fol-

lowing control current:

$$i_u(t) = \frac{1}{r_k}\left\{v_{\mathrm{P}}(t-\Gamma) - v_{\mathrm{P}}(t)\right\}, \tag{9}$$

which is proportional to the difference between the previous voltage with a delay Γ and the present voltage.

The circuit equation can be reduced to a dimensionless nonlinear dynamical system of the following form:

$$\begin{cases} \dot{x} = -\dfrac{a}{x} + by + u \\ \dot{y} = -x - by + 1 \end{cases}, \tag{10}$$

where control signal u is given as

$$u = k\left(x_T - x\right), \tag{11}$$

via the transformations given in Eqs. (2), (3), and the additional transformations,

$$x_T := \frac{1}{E}v_{\mathrm{P}}(t-\Gamma),\ T := \frac{\Gamma}{rC},\ k := \frac{r}{r_k}. \tag{12}$$

The control signal (11) does not change the location of $\boldsymbol{p}_+$ but can change its stability.

The stability of $\boldsymbol{p}_+$ is described by the characteristic quasipolynomial

$$g(s,T) := s^2 + (b-a^*)s + b(1-a^*) + k(s+b)\left(1-e^{-sT}\right), \tag{13}$$

where $a^* := 4a/\left(1+\sqrt{1-4a}\right)^2$. Analysis performed in previous studies [47,48] based on reference [51] yielded the following results.

Theorem 1 ([47,48,51]) *Assume that*

$$b < a^* < 1 \tag{14}$$

holds. If k satisfies the inequalities

$$\begin{aligned} &d_1 := b^2 + a^{*2} - 2b - 2a^*k < 0, \\ &d_2 := d_1^2 - 4b^2(1-a^*)(1-a^*+2k) > 0, \\ &d_3 := \psi_1/\omega_1 - \psi_2/\omega_2 < 0, \end{aligned} \tag{15}$$

where

$$\omega_1 := \sqrt{\frac{-d_1-\sqrt{d_2}}{2}},\ \omega_2 := \sqrt{\frac{-d_1+\sqrt{d_2}}{2}},$$
$$\psi_{1,2} := \mathrm{Arg}\left[\frac{k(b+j\omega_{1,2})}{b(1-a^*+k)-\omega_{1,2}^2 + j\omega_{1,2}(b-a^*+k)}\right],$$

then there exist values of T such that $g(s,T)$ is stable. Here, $\mathrm{Arg}[\mathsf{z}] \in [0,2\pi)$ denotes the principal argument of $\mathsf{z} \in \mathbb{C}$. Furthermore, note that $g(s,T)$ is stable if and only if T falls within one of the following ranges:

$$\begin{aligned} &T \in \left(\frac{\psi_1+2\pi l}{\omega_1}, \frac{\psi_2+2\pi l}{\omega_2}\right), \\ &l = 0, \ldots, \left\lfloor \frac{\psi_2\omega_1 - \psi_1\omega_2}{2\pi(\omega_2-\omega_1)} \right\rfloor, \end{aligned} \tag{16}$$

where $\lfloor \mathsf{r} \rfloor$ represents the largest integer not greater than $\mathsf{r} \in \mathbb{R}$.

This theorem does not state that the controller (11) with k and T designed for a given parameter $a \equiv a_g$ guarantees stability for $a \in (0, a_g]$. Because the definition of a given in Eq. (3) depends on power P and voltage source E, a should be considered an uncertain parameter in real situations. For such situations, our previous study [48] provides the following useful result.

Corollary 1 ([48]) *Assume that k and T in the controller (11) are designed for given values of $a \equiv a_g$ and b on the basis of Theorem 1. If there exists no $\omega > 0$ such that the conditions*

$$f_1(\omega) := \omega^3 + \omega b(b-1) + k(b^2+\omega^2)\sin\omega T = 0, \tag{17}$$

$$f_2(\omega) := \omega(b-a^*) + \omega k(1-\cos\omega T) + bk\sin\omega T < 0 \tag{18}$$

are satisfied, then the operating point $\boldsymbol{p}_+$ in the bus system (10) with the controller (11) is stable for all $a \in (0, a_g]$.

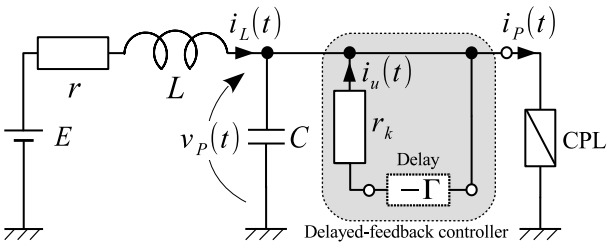


Fig. 7 Delayed feedback controller attached to DC bus system

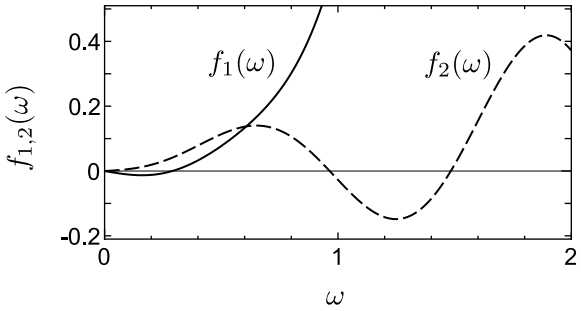


Fig. 8 Functions $f_{1,2}(\omega)$ with $k = 0.17$ and $T = 5$ for $\omega > 0$

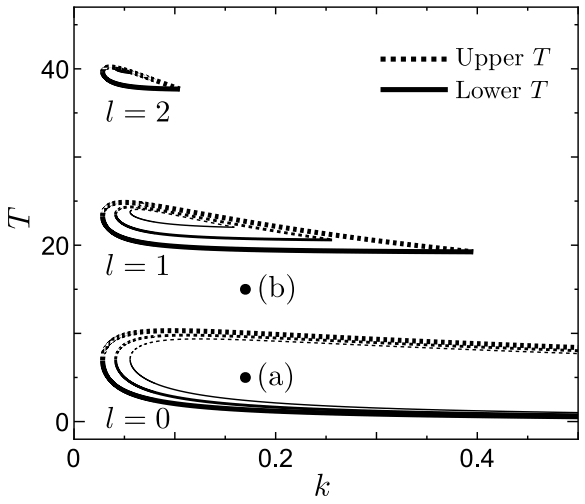


Fig. 9 Stability regions in k–T space defined by upper and lower bounds of T given by Eq. (16) for $b = 0.19$ and $a = 0.18$ (thin lines), 0.17 (normal lines), and 0.16 (thick lines). Dots indicate parameter sets (a) $(k, T) = (0.17, 5)$ and (b) $(k, T) = (0.17, 15)$

A controller with k and T values that satisfy this corollary guarantees the stability of the operating point $\boldsymbol{p}_+$ for all $a \in (0, a_g]$; then, a_g can be considered the upper limit of a.

Corollary 1 is confirmed through a numerical example. The parameter b is fixed at 0.19 and a_g is set to 0.18. Controller parameters k and T are designed based on Theorem 1: $k = 0.17$ and $T = 5$. The functions $f_{1,2}(\omega)$ are plotted in Fig. 8. As shown, there exists no $\omega > 0$ such that both $f_1(\omega) = 0$ and $f_2(\omega) < 0$ are satisfied. Therefore, $\boldsymbol{p}_+$ must be stable for all $a \in (0, a_g]$. Figure 9 shows the upper and lower bounds for T given by Eq. (16) in k–T space with $a = 0.18$, 0.17, and 0.16; the regions bounded by these curves are the stability regions for each set of conditions. The designed k and T corresponding to the dot labeled (a) in Fig. 9 are within the stability region for all $a \in (0, a_g]$ with $a_g = 0.18$. These stability regions reported in [47,48] are experimentally confirmed in the following subsection.

3.2 Experimental results

This subsection reports the circuit implementation of the delayed feedback controller. The stability analysis given in Theorem 1 is confirmed using a real electronic circuit.

3.2.1 Circuit implementation

The DC bus system with the delayed feedback controller is implemented as illustrated in Fig. 7. The controller consists of feedback resistance r_k and a delay unit.

Figure 10 shows a diagram of the delay unit that consists of one delay block and two level-shift blocks. A detailed circuit diagram of this delay unit is shown in Appendix D. The level-shift block on the left side shifts $v_p(t)$, which is the bus line voltage, from a range of 9–20 V to a range of 0–5 V. The other level-shift block shifts a voltage from the range of 0–5 V to the range of 9–20 V. The delay block is implemented by a digital computer with an analog-to-digital (A/D) converter that can deal with the range 0–5 V. The analog-to-digital converter samples the shifted voltage with a sampling period of 25 µs and converts it to digital data. The data are then inserted into a first-in-first-out queue, whose length is proportional to the time delay Γ. The digital data are popped from the queue and converted to an analog voltage by a digital-to-analog (D/A) converter. The voltage shifted to the range of 9–20 V by the level-shift block is applied to feedback resistance r_k as the delayed voltage $v_p(t - \Gamma)$. In this way, the control current $i_u(t)$ in Eq. (9) is injected into the bus line.

3.2.2 Time series data and stability region

The stability analysis given in Theorem 1 is confirmed in this subsection. The circuit parameters are set to $a = 0.16$ and $b = 0.19$. Gain k and delay time T, which are defined in Eq. (12), can be tuned by varying feedback resistance r_k and the length of the queue, respectively. First, k and T are fixed at the values in the stability region mentioned in the preceding subsection: $(k, T) = (0.17, 5)$ ((a) in Fig. 9). The time series data of bus voltage $v_p(t) \propto x(\tau)$ and control current $i_u(t) \propto u(\tau)$ are shown in Fig. 11(a). The circuit state is fixed at $v_P(t) = 15.0\,\mathrm{V}$ and $i_L(t) = 0.133\,\mathrm{A}$ for $t \in [0\,\mathrm{s},\ 0.01\,\mathrm{s}]$. This system begins to work at $t = 0.01\,\mathrm{s}$. As shown in Fig. 11(a), $v_p(t)$ and $i_u(t)$ converge to the operating point and zero, respectively. Then, k and T are set so as not to satisfy Theorem 1: $(k, T) = (0.17, 15)$ ((b) in Fig. 9). The time series data shown in Fig. 11(b) indicate that $v_p(t)$ and $i_u(t)$ do not converge under these operating conditions.

The stability regions in k–T space for $a = 0.18$, 0.17, and 0.16 shown in Fig. 9 are confirmed through circuit experiments. Figures 12(a), 12(b), and 12(c) show controller parameters k and T at which a stable operating point is or is not experimentally observed. The experimental results shown in Fig. 12 agree well with the analytical results in Fig. 9.

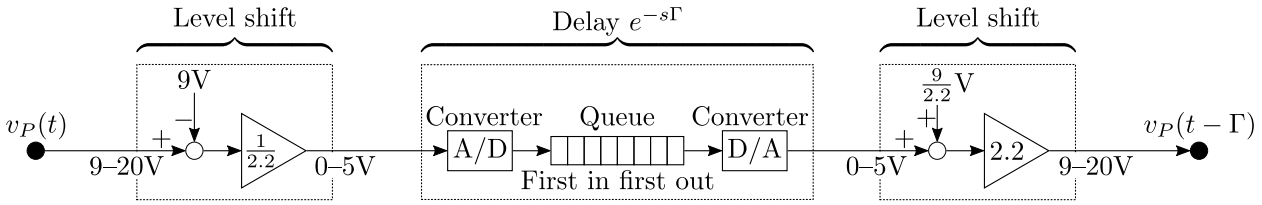
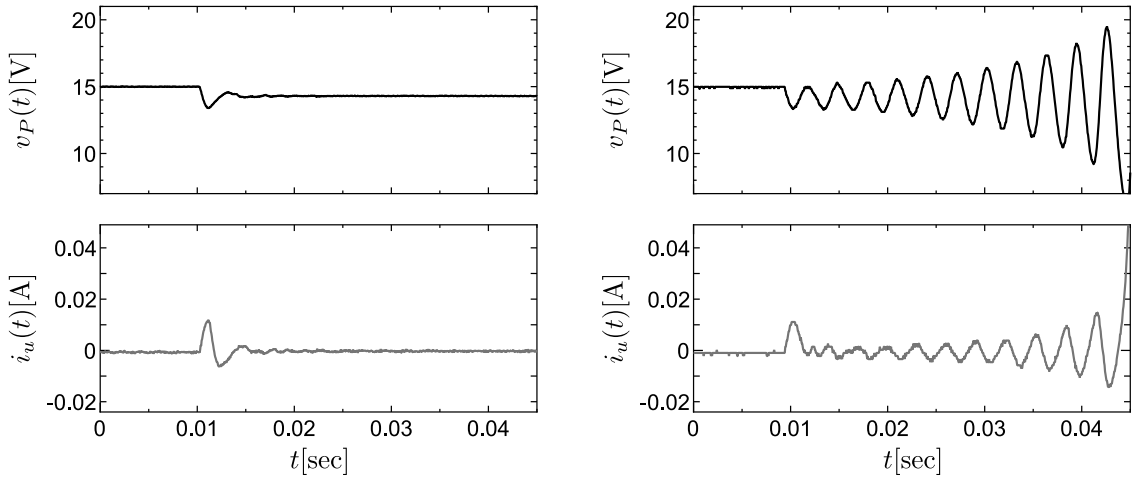
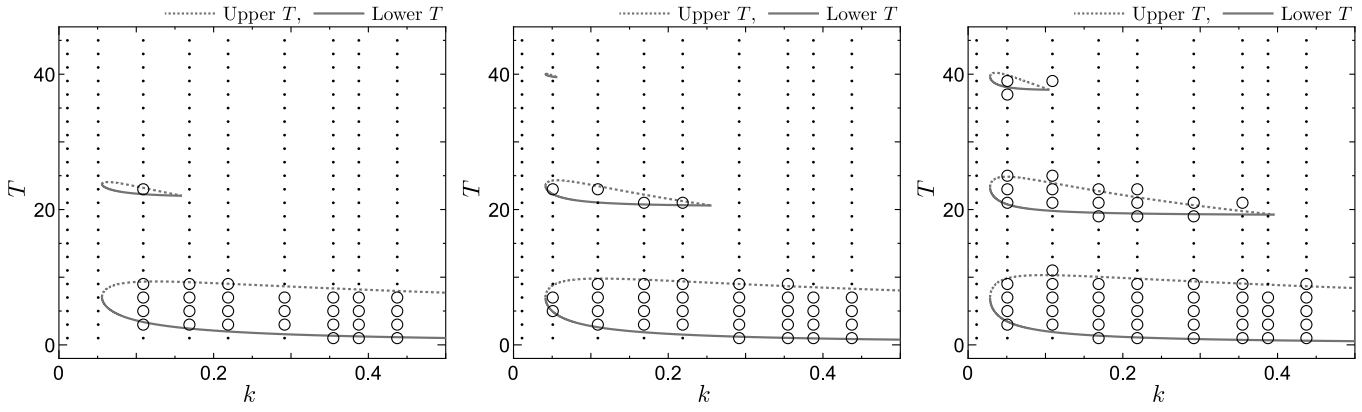


Fig. 10 Diagram of delay unit



(a) $(k, T) = (0.17, 5)$ (b) $(k, T) = (0.17, 15)$

Fig. 11 Experimental time series data of bus voltage $v_p(t)$ and control current $i_u(t)$ with $a = 0.16$ and $b = 0.19$. Circuit state is fixed at $v_P(t) = 15.0\,\mathrm{V}$ and $i_L(t) = 0.133\,\mathrm{A}$ for $t \in [0\mathrm{s},\ 0.01\mathrm{s}]$. This system begins to work at $t = 0.01\,\mathrm{s}$



(a) $a = 0.18$ (b) $a = 0.17$ (c) $a = 0.16$

Fig. 12 Experimental verification of controller parameters k and T inducing stabilization for $a = 0.18$, 0.17, and 0.16. Circles and dots indicate controller parameter sets (k, T), where the operating point is experimentally found to be stable and unstable, respectively

4 Tracking performance

From a practical point of view, it is likely that power consumption P will vary with time due to changes in user demands. This section analytically and experimentally examines this situation.

4.1 Slow and rapid changes in power consumption

Our previous study [47] reported numerical simulations where delayed feedback control was successfully used to track operating point $\boldsymbol{p}_+(\tau)$ even when power consumption P was slowly varied with time. In the present study, the practical situation is experimentally consid-

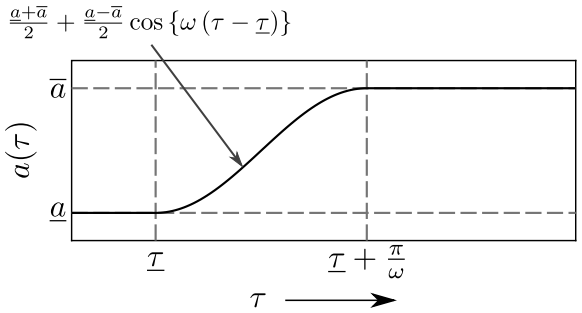


Fig. 13 Illustration of change in $a(\tau)$ described by Eq. (20)

ered with the parameters

$$b = 0.19,\ k = 0.11,\ T = 5. \tag{19}$$

According to Eqs. (4) and (5), if P varies with time, operating point $\boldsymbol{p}_+(\tau)$ also varies with time. In the present circuit experiments, P is varied by controlling the voltage $e(t)$ of the CPL circuit in Fig. 3 (see Eq. (8)). This variation corresponds to the following ramped increase of $a(\tau)$ from lower limit $\underline{a}$ to upper limit $\overline{a}$:

$$a(\tau) = \begin{cases} \underline{a} & \tau < \underline{\tau} \\ \dfrac{\underline{a}+\overline{a}}{2} + \dfrac{\underline{a}-\overline{a}}{2}\cos\{\omega(\tau-\underline{\tau})\} & \tau \in \left[\underline{\tau}, \underline{\tau}+\dfrac{\pi}{\omega}\right] \\ \overline{a} & \tau > \underline{\tau}+\dfrac{\pi}{\omega} \end{cases}, \tag{20}$$

as illustrated in Fig. 13. The frequency ω represents how rapidly a changes from $\underline{a}$ to $\overline{a}$. Here, the lower and upper limits of a and the time window parameter are set to $\underline{a} = 0.145$, $\overline{a} = 0.190$, and $\underline{\tau} = 25$.

Cases with slowly and rapidly changing $a(\tau)$, corresponding to $\omega = 0.05$ and $\omega = 0.70$, respectively, are considered. Figures 14(a) and 14(b) show the time series data of $a(\tau)$, circuit state $x(\tau)$, and operating point $x^*_+(\tau)$ for the slow ($\omega = 0.05$) and rapid ($\omega = 0.70$) changes, respectively. The parameter $a(\tau)$ is estimated from voltage $e(t)$ and Eqs. (3) and (8). Circuit state $x(\tau)$ is obtained from the measured voltage $v_{\mathrm{P}}(t)$ and Eq. (2). Operating point $x^*_+(\tau)$ is calculated from the estimated $a(\tau)$ and Eq. (5). As shown in Fig. 14(a), in the slow change case ($\omega = 0.05$), $a(\tau)$ and $x^*_+(\tau)$ change slowly, and $x(\tau)$ successfully tracks $x^*_+(\tau)$. In contrast, as shown in Fig. 14(b), in the rapid change case ($\omega = 0.70$), $x(\tau)$ fails to track $x^*_+(\tau)$ despite operating point $\boldsymbol{p}_+(\tau)$ remaining stable. These results suggest that $x(\tau)$ can track $x^*_+(\tau)$ for slow changes in power but not for rapid changes.

4.2 Frequency domain analysis

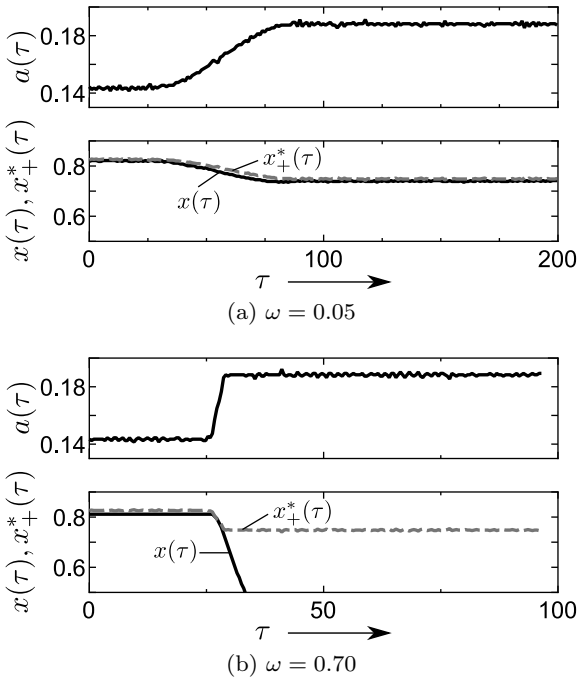


Fig. 14 Experimental time series data for $a(\tau)$, $x(\tau)$, and $x^*_+(\tau)$ under (a) slow variation ($\omega = 0.05$) and (b) rapid variation ($\omega = 0.70$)

From a practical point of view, it is crucial to analytically obtain the criterion for the variation frequency. To this end, the present study utilizes frequency domain analysis. The small perturbation of $a(\tau)$ around the nominal value $a_0 > 0$ is defined as

$$a_{\Delta}(\tau) := a(\tau) - a_0. \tag{21}$$

Here, we define the operating point $\boldsymbol{p}_+(\tau)$ at $a = a_0$ as $\boldsymbol{p}_{+0} := [x^*_{+0}, y^*_{+0}]^T$. The perturbation $a_{\Delta}(\tau)$ induces the operating point perturbation $\Delta x^*_+(\tau) := x^*_+(\tau) - x^*_{+0}$. The perturbations of the circuit state variables are then defined as

$$\begin{aligned} \begin{bmatrix} x_{\Delta}(\tau)\ y_{\Delta}(\tau) \end{bmatrix}^{\mathrm{T}} &:= \begin{bmatrix} x(\tau)\ y(\tau) \end{bmatrix}^{\mathrm{T}} - \boldsymbol{p}_{+0}, \\ \begin{bmatrix} x_{\Delta T}(\tau)\ y_{\Delta T}(\tau) \end{bmatrix}^{\mathrm{T}} &:= \begin{bmatrix} x_T(\tau)\ y_T(\tau) \end{bmatrix}^{\mathrm{T}} - \boldsymbol{p}_{+0}. \end{aligned} \tag{22}$$

The dynamics of these perturbations around the operating point $\boldsymbol{p}_{+0}$ are approximately obtained by linearizing the system given in Eq. (10) as

$$\begin{aligned} \frac{\mathrm{d}}{\mathrm{d}\tau}\begin{bmatrix} x_{\Delta}(\tau) \\ y_{\Delta}(\tau) \end{bmatrix} &= \begin{bmatrix} -k + a_0/(x^*_{+0})^2 & b \\ -1 & -b \end{bmatrix}\begin{bmatrix} x_{\Delta}(\tau) \\ y_{\Delta}(\tau) \end{bmatrix} \\ &+ \begin{bmatrix} k & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} x_{\Delta T}(\tau) \\ y_{\Delta T}(\tau) \end{bmatrix} + \begin{bmatrix} (2x^*_{+0}-1)/x^*_{+0} \\ 0 \end{bmatrix}\Delta x^*_+(\tau). \end{aligned} \tag{23}$$

The influence of Δx^*_+ on x_{Δ} can be described by

$$x_{\Delta} = G(s)\Delta x^*_+, \tag{24}$$

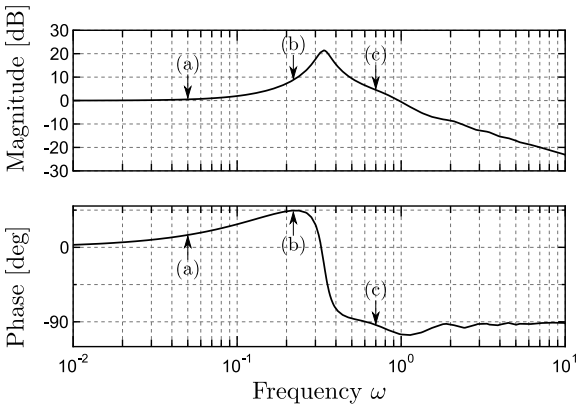


Fig. 15 Bode plot for $G(s)$ ($a_0 = 0.18$, $b = 0.19$, $k = 0.11$, $T = 5$). Arrows indicate the magnitude and the phase with (a) $\omega = 0.05$, (b) $\omega = 0.22$, and (c) $\omega = 0.70$

where $G(s)$ is the transfer function, defined as

$$G(s) := \frac{(s+b)(2x^*_{+0} - 1)/x^*_{+0}}{g(s,T)}. \tag{25}$$

Figure 15 shows a Bode plot for $G(s)$ with the parameters defined as given in Eq. (19) and $a_0 = 0.18$. The magnitude in the upper graph is $20\log|G(j\omega)|$, which represents the ratio of the x_Δ magnitude to the Δx^*_+ magnitude. The phase in the lower graph is $\angle G(j\omega)$, which represents the difference in phase between x_Δ and Δx^*_+. Figure 15 provides three pieces of useful information on the tracking performance of the controller (11). First, for $\omega \leq 0.09$, the magnitude satisfies $20\log|G(j\omega)| \leq 1.6\,\mathrm{dB}$, and the phase is in the range $\angle G(j\omega) \in (0°, 25.6°)$; the amplitude and phase of x_Δ are almost equal to those of Δx^*_+. This fact shows that $x(\tau)$ successfully tracks $x^*_+(\tau)$ for $\omega \leq 0.09$. Second, at resonant frequency $\omega = 0.34$, the magnitude is 21.4 dB. This indicates that the amplitude of x_Δ is much larger than that of Δx^*_+ for frequencies approaching $\omega = 0.34$. Third, for $\omega > 0.34$, the phase is about $-90°$. In this range, the phase of x_Δ is quite different from that of Δx^*_+. This information on the tracking performance is useful for designing the controller (11) and restricting the change rate of power consumption.

The analytical results for the three frequency ranges described above are confirmed through circuit experiments. The parameters are set to the values given in Eq. (19), and $a(\tau)$ is varied as

$$a_0 = 0.18,\ a_\Delta(\tau) = 0.01\sin\omega\tau. \tag{26}$$

Figures 16(a), 16(b), and 16(c) show the time series data of $a(\tau)$, $x(\tau)$, and $x^*_+(\tau)$ for $\omega = 0.05$, 0.22, and 0.70, respectively (see arrows (a), (b), and (c) in Fig. 15). These values respectively satisfy the first condition of $\omega < 0.09$, the second condition of ω approaching the resonant frequency $\omega = 0.34$, and the third condition of $\omega > 0.34$, as discussed above. For $\omega = 0.05$ (Fig. 16(a)), $x(\tau)$ successfully tracks $x^*_+(\tau)$. For $\omega = 0.22$ (Fig. 16(b)), the amplitude of $x(\tau)$ is larger than that of $x^*_+(\tau)$; thus $x(\tau)$ fails to track $x^*_+(\tau)$. For $\omega = 0.70$ (Fig. 16(c)), $x(\tau)$ fails to track $x^*_+(\tau)$ because of a large phase difference. These experimental results agree with the analytical results presented above.

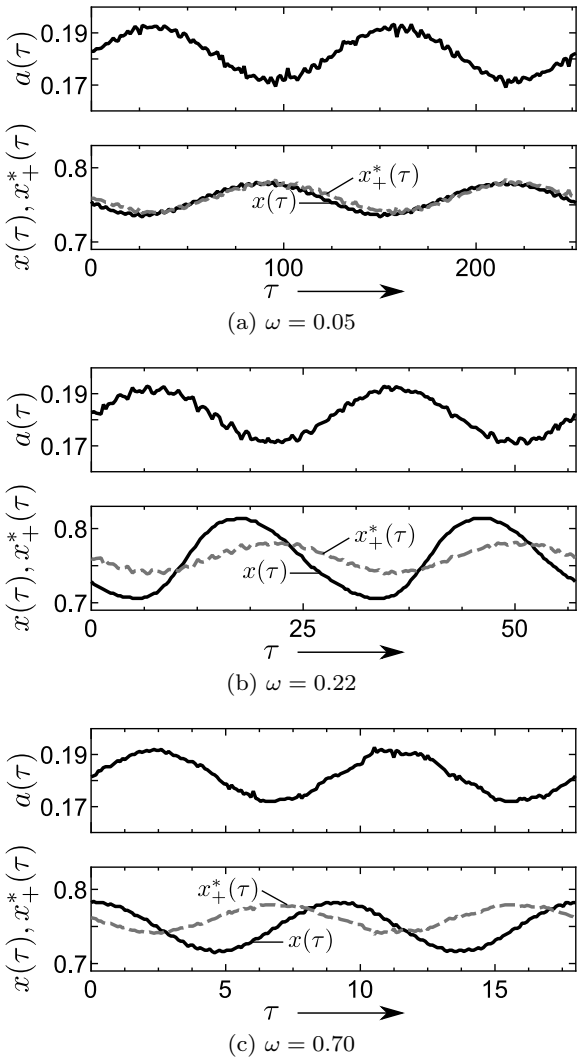


Fig. 16 Experimental time series data for $a(\tau)$, $x(\tau)$, and $x^*_+(\tau)$ with (a) $\omega = 0.05$, (b) $\omega = 0.22$, and (c) $\omega = 0.70$

The analytical and experimental results indicate that the frequency domain analysis revealed the relationship between the controller parameters (k, T) and the frequency ω of the CPL. This relationship can be used in two ways. First, for a given parameter set (k, T), the upper limit of ω under which the controller successfully tracks the operating point can be estimated; second, given the upper limit of ω, the parameters (k, T) can

be selected such that the resonant frequency is much higher than the upper limit.

5 Conclusion

This study experimentally investigated the dynamics of a DC bus system without control and with delayed feedback control. Three main contributions of this study are seen in the results. First, analytically derived Hopf and saddle-node bifurcation scenarios in a DC bus system without control were experimentally confirmed. Second, the behavior of a real DC bus system with a delayed-feedback digital circuit controller agreed well with the analytical results. It was also experimentally confirmed that the controller can track an operating point that varies slowly, but not rapidly, with time due to changes in power consumption. Third, it was found that frequency-domain analysis provides useful information on the tracking performance of the controller. This information can be utilized in the following two ways: for a given delayed feedback controller, the upper limit of the acceptable power consumption rate of change can be estimated in advance; for a given upper limit, the controller parameters can be selected so as to successfully track it. In addition, we experimentally confirmed that frequency-domain analysis is a practical tool for evaluating tracking performance. The above results confirm that delayed feedback control, which is a popular scheme for stabilizing chaotic systems in the field of nonlinear science, has potential to be utilized for stabilizing DC bus systems.

Acknowledgements This study was partially supported by JSPS KAKENHI (JP26289131, JP18H03306).

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

Appendix A: Comparison to adaptive techniques

Derivative control and low-/high-pass first-order RC filter techniques can also track the operating point. However, derivative control is sensitive to high-frequency noise in practical situations, because its control law requires differentiation. Moreover, low-/high-pass first-order RC filter techniques require an additional large capacitor (e.g., an electrolytic capacitor) to stabilize the system. In general, capacitors have a high maintenance cost and reduce the lifetime of power electronic equipment [52,53]. In contrast, delayed feedback control requires neither differentiation [54] nor capacitors.

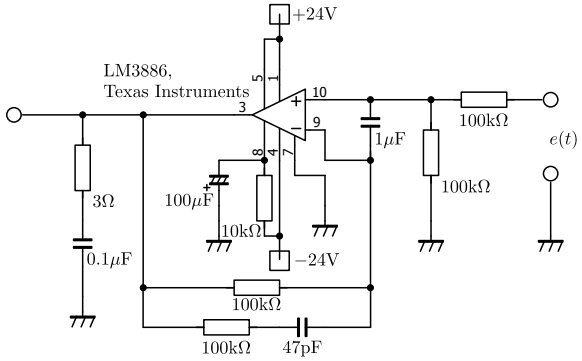


Fig. 17 Circuit diagram of amplifier connected to R_L in CPL circuit

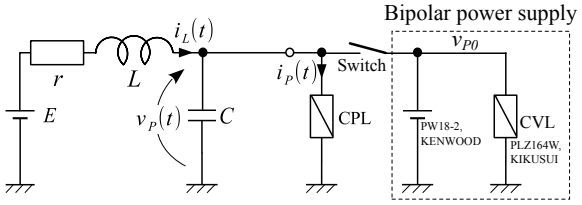


Fig. 18 Bipolar power supply connected to DC bus line to set initial voltages

Appendix B: Amplifier in CPL

A circuit diagram of an amplifier connected to load resistance R_L in the CPL circuit (see Fig. 3) is shown in Fig. 17, where the main device is an audio power amplifier (LM3886, Texas Instruments).

Appendix C: Experimental procedure for setting initial points

This appendix describes the experimental procedure used for setting the initial points $v_P(0)$ ($\Leftrightarrow x(0)$) and $i_L(0)$ ($\Leftrightarrow y(0)$). To set these points to the desired voltage and current, a bipolar power supply, which consists of a standard DC power supply (PW18-2, KENWOOD) and a constant voltage load (CVL) (PLZ164W, KIKUSUI), is connected to the bus line as illustrated in Fig. 18. When the switch is closed, the initial bus voltage is fixed at $v_P(0) = v_{P0}$, where v_{P0} can be set to the desired value. The initial bus line current depends on v_{P0}, $i_L(0) = (E - v_{P0})/r$; thus, these initial points are on the nullcline $\dot{y} = 0$. When the switch is opened, the DC bus system starts from the initial voltage and current.

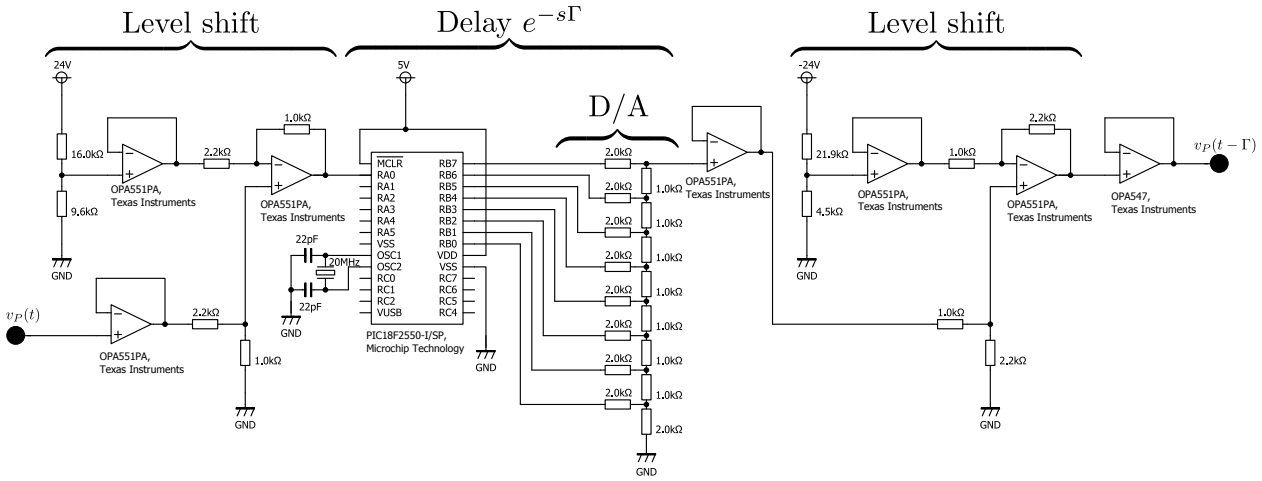


Fig. 19 Circuit implementation of delay unit

Appendix D: Digital implementation of delay unit

The circuit of the delay unit is shown in Fig. 19. In this unit, a peripheral interface controller (PIC; PIC18F2550-I/SP, Microchip Technology) is used as a digital computer. Voltage $v_p(t)$ is applied to the level-shift circuit, which shifts the voltage range of $v_p(t)$ to the range 0–5 V, since the PIC can deal with this range. The shifted voltage is sent to the input terminal RA0 of an analog-to-digital converter built into the PIC and transformed into a digital data. The received data are delayed using the first-in-first-out rule program on the PIC. The delayed voltage signal is sent to the output terminals RB0, RB1,..., RB7 and transformed into an analog voltage by a digital-to-analog converter (R-2R ladder). The delayed analog voltage is transformed into a voltage in the original voltage range by a differential amplifier. The delayed voltage $v_p(t-\Gamma)$ is applied to feedback resistance r_k. The control current $i_u(t)$ in Eq. (9) is injected into the bus line.

The PIC has an analog-to-digital converter with 8-bit resolution and a sampling period of 25 µs. The voltage resolution (0.043 V) is just 0.24% of the source voltage E; the sampling period (25 µs) is about 1% of the natural period of the operating point. This resolution and this period are small and short enough for the digital controller to be used as an ideal analog controller.

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