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Photonic Crystal Nanocavities with an Average Q factor of 1.9 million Fabricated on a 300-mm-Wide SOI Wafer Using a CMOS-Compatible Process

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Abstract— **Electron-beam lithography allows precise photonic crystal (PC) fabrication, but is not suitable for mass production. Therefore, the development and optimization of CMOS-compatible processes is necessary to implement unique nanocavity technologies in optoelectronic circuits. We investigated the quality factors (Q) and the resonant wavelengths (λ) of PC heterostructure nanocavities fabricated by the 193-nm argon fluoride immersion lithography on a 300-mm-wide silicon-on-insulator wafer. We measured thirty cavities distributed over nine chips at various positions of the wafer. An average Q of 1.9 million was obtained for the thirty cavities, and the highest value was 2.5 million, which is the highest Q reported so far for a nanocavity fabricated by photolithography. Such high Q were realized by the improvements of the nanocavity design and the fabrication process. All nanocavities exhibited a Q of larger than 1 million and the fluctuation of the chip-averaged Q was independent of the chip location. On the other hand, the measured λ tended to shift to shorter wavelengths as the distance between the nanocavity and the substrate center increased. Among the nine chips, the difference of the chip-averaged λ was as large as 8.0 nm. We consider that a systematic shift of the average air-hole radius by several nanometers is responsible for the large fluctuation of the chip-averaged λ. These statistical studies provide important hints to accelerate the application study of PC high-Q nanocavities.**

Index Terms—**photonic crystal, SOI wafer, photolithography, resonator, fabrication process**

I. INTRODUCTION

NANOCAVITIES based on artificial defects in two-dimensional (2D) photonic crystal (PC) slabs have

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attracted much attention because they combine a high-quality factor (high-Q) with a small modal volume that approaches one cubic wavelength [1-6]. In particular, several types of nanocavities fabricated on silicon-on-insulator (SOI) wafers have achieved high experimental Q exceeding 1 million [7-14]. Such ultrahigh-Q nanocavities enable unique devices for optical circuits, e.g. optical pulse traps with dynamic control [15-17], two photon absorption photodiodes with low operating energies [18], and ultralow-threshold Raman Si lasers [19-21].

Recently, the integration of optical links using silicon (Si) photonics attracts attention as a technology to reduce the power consumption related to information transport via electrical wiring in huge data centers [22-24]. The sizes of the PC ultrahigh-Q nanocavities are more than one order of magnitude smaller than those of the ultrahigh-Q Si ring resonators [25, 26]. Therefore, ultrahigh-Q nanocavities are expected to contribute to the development of optical wiring based on Si photonics. Research on the mass production of ultrahigh-Q nanocavities with a complementary metal–oxide–semiconductor (CMOS)-compatible process is important.

The experimentally determined Q (Q_{exp}) for a heterostructure nanocavity with an ideal Q (Q_{ideal}) greater than 10 million can easily drop below 1 million due to random nanometer-scale variations in the air hole geometry, which forms the PC nanocavity [27]. Previous studies have clarified that the variations in the radii and positions of the air holes should not exceed a standard deviation of 1 nm in order to fabricate ultrahigh-Q nanocavities with a Q_{exp} larger than 1 million [28, 29]. Accordingly, high accuracy is indispensable for the lithography process that defines the PC pattern. Therefore, ultrahigh-Q nanocavities have so far been fabricated with electron-beam (EB) lithography, which is not preferable for mass production due to the slow EB lithography process. Very recently, we have reported nanocavities with an average Q_{exp} of 1.5 million fabricated by a CMOS process with argon fluoride (ArF) immersion photolithography [30]. In this previous study, we reported the experimental results for one specific chip located 50 mm away from the center of the 300-mm-wide wafer. However, for industrial applications it is important to fabricate ultrahigh-Q nanocavities at any position of the wafer. In addition, besides the Q values, also the resonant wavelength (λ)

of the nanocavity is important for optical wiring technologies [31, 32]. The experimentally obtained λ (λ_{exp}) is not only determined by the magnitude of the random fluctuation in the air hole dimensions with respect to the average geometry, but also by an overall shift in the average radius and the thickness of the PC slab. Therefore, λ_{exp} should show a different dependence on the wafer position than Q_{exp}, because the latter is independent of changes in the slab thickness and average radius on the order of 1%.

In this study, we determined the Q_{exp} and λ_{exp} of thirty heterostructure nanocavities that are distributed over the nine chips at various positions of the 300-mm-wide SOI wafer. In order to increase the Q_{exp}, we improved the design of the nanocavity sample and the fabrication process. All measured thirty nanocavities exhibited a Q_{exp} larger than 1 million. The average Q_{exp} value of the thirty cavities was 1.9 million and the highest value was 2.5 million. Although the Q_{exp} values fluctuated as a result of the random air hole imperfections, the fluctuation of the chip-averaged Q_{exp} was independent of the chip location. From a numerical simulation, the standard deviation of air hole size variations (σ_{hole}) that is responsible for the fluctuation of Q_{exp} was estimated to be 0.57 nm. On the other hand, the difference between the chip-averaged λ_{exp} was as large as 8.0 nm, which was much larger than the fluctuation of λ within any chip. Furthermore, the measured λ_{exp} tended to shift to shorter wavelengths as the distance between the nanocavity and the substrate center increased. These results cannot be explained by the evaluated σ_{hole}, which is only on the sub-nanometer scale. The analytical study indicated that the main cause is the systematic change in average radius of the air holes, which depends on the chip location relative to the substrate center.

II. Sample structure and Fabrication Method

Figure 1 shows an overview of the heterostructure nanocavity sample studied in this work. We utilized a 300-mm-wide SOI wafer with a buried oxide (BOX) layer that had a thickness of 3 µm. The thickness of the PC slab was about 220 nm. The maximum difference in the thickness for 300-mm-wide wafer was 1.9 nm in the inspection data. The PC consisted of a triangular lattice of circular air holes. The radii were about 113 nm for the chips close to a center of the substrate (see Table II), which was estimated via scanning electron microscopy (SEM) (Figure 1(b); SEM image of the actual sample). The heterostructure nanocavity was formed by a line defect of 23 missing air holes. Four different lattice constants were used to form the nanocavity. The lattice constant in the y-direction was W_1 = 710 nm. To obtain confinement with a double-heterostructure, the lattice constants in the x-direction were symmetrically increased for the three pairs of lines at the center of the cavity [4]. As shown in Figure 1(b), the lattice constants of the resulting central, intermediate and outer regions were 418 nm, 414 nm, and 410 nm, respectively. The Q_{ideal} and ideal resonant wavelength (λ_{ideal}) of the nanocavity mode were 3.3×10^7 and 1577.0 nm, respectively, as calculated by the three-dimensional (3D) finite difference time domain (FDTD) method (Figure 1(d);
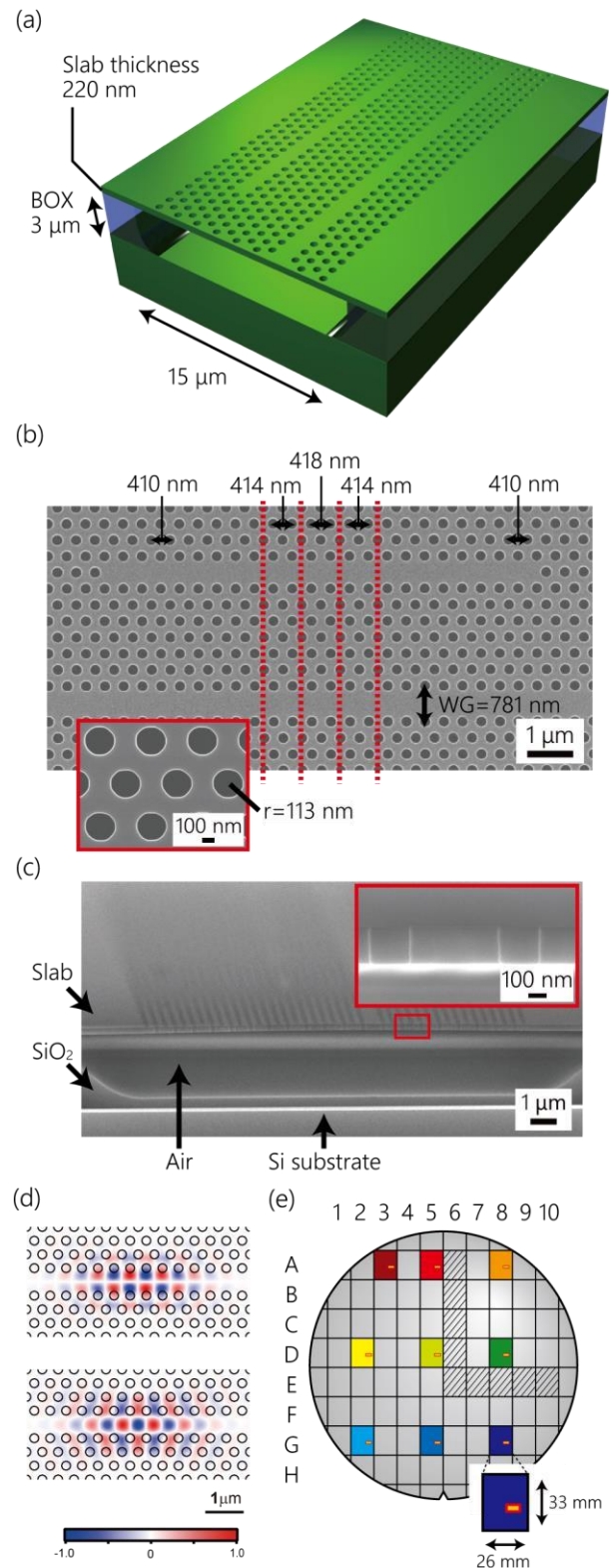

Fig. 1. (a) Illustration of the heterostructure nanocavity. (b) SEM image of the fabricated sample. (c) Cross-sectional SEM image of the PC slab. The magnified image indicates the tilt of the holes. (d) Calculated x-component (upper) and y-component (lower) of the electric field distribution. They are normalized by the maximum value for each distribution. (e) Arrangement of the 60 chips on the 300-mm-wide SOI wafer. Colored areas indicate the positions of the chips that were used in the measurements. Hatched chips were used to investigate the systematic shift of radius. Small square in each chip roughly represents the pattern position for the four heterostructure nanocavities. The remaining area was used for other silicon photonics devices.

calculated electric field distributions). The excitation waveguide adjacent to the cavity was 10% wider in the y-direction (i.e., $1.1W_1$), and the separation from the cavity was eight rows of air holes. These waveguide width and distance were chosen to significantly reduce the loads of the waveguides to Q_{exp} (see Sec. IV.A). The excitation waveguide extends to the edge of the chip and is used to couple light into the cavity. The geometry of the nanocavity was the same as that for our previous report except for the shift of the lattice constant and the thickness of the BOX layer [30]. The shift to form the double-heterostructure was decreased from 5 to 4 nm, which increase the Q_{ideal} from 2.1×10^7 to 3.3×10^7. The thickness of the BOX layer was increased from 2 to 3 μm to increase the optical confinement due to the air-bridge structure, which will reduce the light leakage from the nanocavity to the substrate side. From these improvements, we can expect the increase of the Q_{exp}.

The photolithography and plasma etching to form air hole structure were performed using CMOS-compatible machinery in the research and development laboratory at AIST. We used an ArF immersion scanner (Nikon NSR-S610C) for 45-nm node volume production. The wavelength of the ArF excimer laser was 193 nm. Purified water was introduced between the projection lens and the resist-coated wafer to increase the numerical aperture (NA) [33]. The short wavelength and large NA resulted in a high resolution, which is important to obtain a random variation in the air hole geometry of less than 1 nm. In addition, we used a half-tone photomask to improve the resolution [34]. The shot size of the photomask was 104 mm × 132 mm which was projected onto the SOI wafer by reducing it to 26 mm × 33 mm, i.e., one quarter in size (the patterns for the heterostructure nanocavities occupies only a part of the chip area). Thus, the lithography pattern formed on a 300-mm-wide SOI consisted of about 60 equivalent chips. Then, the pattern was developed and transferred to the top Si layer by dry etching. The dry-etching recipe was improved to reduce the tilt of the air holes, which is very important to increase the Q_{exp} [27]. The tilt in the previous report was 3.0°. Figure 1(c) provides a cross-sectional SEM image of the fabricated sample, which confirms that the average tilt was less than 2.5°.

Figure 1(e) shows the arrangement of the 60 chips on the 300-mm-wide SOI wafer. Each chip is identified by a row index (A~H) and a column number (1~10). The V-shaped cutout drawn on the wafer is the wafer notch indicating the [110] direction of the Si crystal. For the measurements, we chose nine chips whose positions are indicated with the colored areas in Fig. 1(e). Automated system to measure the properties of the high-Q nanocavities have not been developed and thus, it was difficult to measure all 60 chips. After the wafer was cut into about 60 chips, the following processes were performed using our small-scale fabrication technologies. Each of the nine selected chips was polished to a thickness of 100 μm and cut into a piece with dimensions of 1 mm × 300 μm, in which the heterostructure nanocavities were included. The edges of the piece are along to [110] or equivalent direction. The pieces were bonded to small cubic blocks for optical measurements. Finally, the BOX layer underneath the PC pattern was
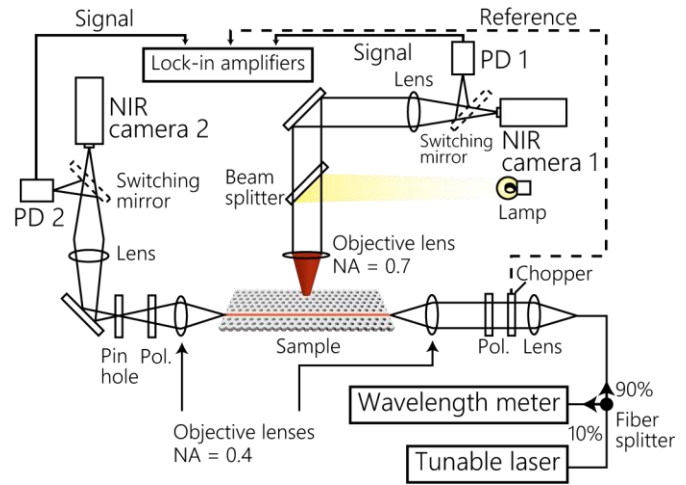

Fig. 2. Setup for measuring the resonance spectra of nanocavities. PD: photodiode, Pol.: polarizer, NA: numerical aperture.

selectively removed by a 48% hydrofluoric acid at room temperature, which resulted in the air-bridge structure.

III. EXPERIMENTAL SETUP

The Q and λ values are determined from the resonance spectra of the nanocavities. Figure 2 shows the measurement setup to obtain the resonance spectra. The light from a continuous-wave tunable laser (Santec TSL-510) was split into two beams. One beam was analyzed by a high-precision wavelength meter with a differential accuracy of ±0.15 pm (Agilent 86122A). The other beam was modulated by a mechanical chopper at a frequency of ~1 kHz and passed through a polarizer to obtain transverse-electric (TE) polarization. This light was focused by an objective lens (NA = 0.4) on the facet of the excitation waveguide to pump the system. The experiment was performed at room temperature in ambient air with a relative humidity of 30 percent. The sample was placed on a high-precision six-axis stage, and the sample temperature was stabilized by using a Peltier element. Since each nanocavity is slightly different, the wavelength of the pump laser has to be scanned for each sample. When the incident wavelength matched λ of the nanocavity, a part of the pump light was extracted by the nanocavity and emitted in the direction perpendicular to the slab. The emitted light was collected by another objective lens (NA = 0.7, Mitutoyo NIR HR 100X) placed on a three-axis stage. The position of the lens was adjusted by using a near-infrared (NIR) camera (FLIR SC2500) so that the emitted light was incident on the InGaAs photodiode (New Focus 2011) (PD1 in Fig. 2). We improved the NA of the objective lens from the previous study, which enabled us to efficiently measure thirty nanocavities. A lamp was used during the position alignment, but it was switched off during the measurement. The pump light that was transmitted through the excitation waveguide was similarly collected by an objective lens with NA = 0.4 and detected by the photodiode PD2. Here, a pin hole was inserted to eliminate the background light. To obtain the resonance spectra, the intensities of the emitted and transmitted lights were measured with a lock-in amplifier system (NF Corporation LI5630) as a function of the
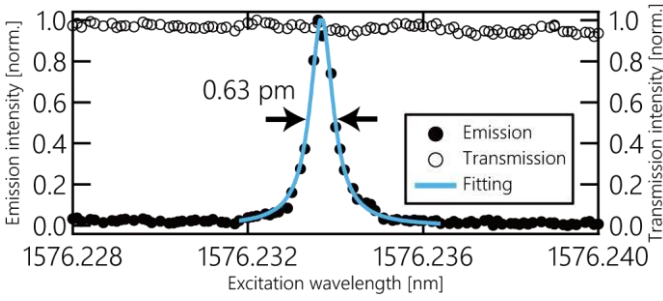
Fig. 3. Emission (filled circles) and transmission (open circle) resonance spectra for the heterostructure nanocavity with the highest Q_{exp} (sample D4_4; $Q_{exp} = 2.50$ million). The solid curve is the fitting result using a Lorentzian function.

TABLE I
THE EXPERIMENTAL Q AND λ OF THE 36 NANOCAVITIES WITH SAME DESIGN

	1	2	3	4
A3		1.79×10^6	1.81×10^6	2.15×10^6
		1574.197 nm	1574.679 nm	1575.628 nm
A5		1.64×10^6	1.59×10^6	
		1573.604 nm	1574.220 nm	
A8	1.14×10^6		1.14×10^6	1.33×10^6
	1573.955 nm		1573.877 nm	1573.584 nm
D2	1.93×10^6	1.54×10^6	2.02×10^6	2.10×10^6
	1576.602 nm	1577.381 nm	1578.150 nm	1578.576 nm
D5	2.38×10^6	2.18×10^6	2.03×10^6	2.50×10^6
	1575.672 nm	1575.860 nm	1575.693 nm	1576.233 nm
D8		1.84×10^6	2.01×10^6	1.59×10^6
		1577.474 nm	1578.006 nm	1577.790 nm
G2	2.11×10^6	1.99×10^6	1.55×10^6	2.33×10^6
	1569.186 nm	1569.420 nm	1569.552 nm	1570.695 nm
G5	1.88×10^6	2.08×10^6	1.65×10^6	2.39×10^6
	1575.463 nm	1574.661 nm	1573.732 nm	1574.724 nm
G8	2.00×10^6		1.67×10^6	2.24×10^6
	1571.655 nm		1572.752 nm	1573.297 nm

The row indicates the chip number and the column presents the cavity number of each chip.

excitation laser wavelength.

IV. RESULTS

A. Results for the nine chips

For each of the nine chips, we measured 4 heterostructure nanocavities, which had the same design as shown in Fig. 1(b). Figure 3 shows the emitted (filled circle; measured with PD1) and transmitted (open circle; measured with PD2) resonance spectra for the nanocavity with the highest Q_{exp} among the 36 cavities. The emitted resonance spectrum was fitted using a Lorentzian function (solid curve) and we obtained a full width at half-maximum ($\Delta\lambda$) of 0.63 pm. The effective Q (Q_{load}) value of the nanocavity, which includes the load of the excitation waveguide, was determined with the following relationship:

$$Q_{load} = \lambda_{exp} / \Delta\lambda \tag{1}$$

Here, λ_{exp} is the resonant wavelength obtained from Fig. 3 (1576.234 nm), and thus we obtain $Q_{load} = 2.50 \times 10^6$. From coupled mode theory, Q_{exp} (i.e., the intrinsic Q of the measured cavity excluding the load of the excitation waveguide) can be expressed as follows [35, 36]:
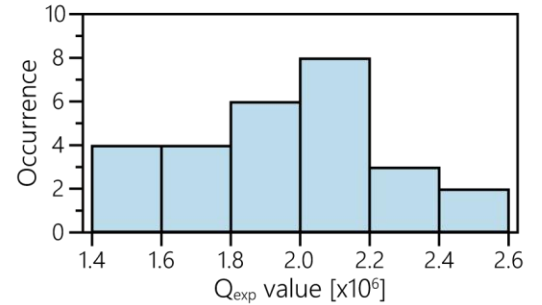
(a)

(b)
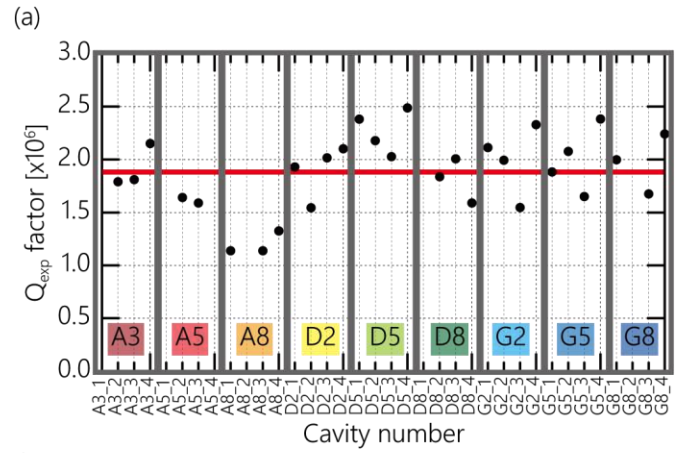
Fig. 4. (a) The experimental Q of the thirty measured nanocavities on the nine chips. The red solid line indicates the average value. (b) Histogram for the thirty cavities except those on chip A8.

$$Q_{exp} = Q_{load} / \sqrt{T_0} \tag{2}$$

T_0 is the transmittance at λ_{exp}. It was almost unity for the cavity shown in Fig. 3, which means that the coupling efficiency between the excitation waveguide and the nanocavity was small (the slightly smaller transmittance for longer wavelengths is a result of Fabry-Pérot oscillation of the excitation waveguide). By using $T_0 = 1.0$, a Q_{exp} value of 2.50 million was obtained for the nanocavity 4 on chip D5 (hereafter referred to as D5_4), which is the highest Q_{exp} reported so far for a nanocavity fabricated by photolithography [14,30,37]. This record was achieved by the improvements of the sample design and the tilt of the hole described in Sec. II. Using the sample with the small coupling, we can investigate the intrinsic Q without an uncertainty (estimation of T_0 has some uncertainty due to the Fano effect and the Fabry-Pérot oscillation [38,39]). On the other hand, it increases the difficulty of the spectral measurement since the emission from the cavity become small. We did not find the emission for six cavities due to a too small coupling. The efficiency can be increased by decreasing the separation between the cavity and the waveguide, which is necessary for the application.

Table 1 summarizes the Q_{exp} and λ_{exp} for the 30 measured nanocavities, which are labelled by the chip number (rows) and the cavity number (columns). As will be discussed in the following sections, the measured values of Q_{exp} and λ_{exp} fluctuated due to random and systematic imperfections of the air holes and the slab thickness.

B. Discussion of the Q_{exp} fluctuation

Figure 4(a) shows the distribution of the Q_{exp} derived from the resonance spectra. The highest Q_{exp} (2.50 million) was obtained for cavity D5_4 while the lowest were those for A8_1 and A8_2 (1.14 million). The red solid line in Fig. 4(a) indicates the average Q_{exp} value for the thirty nanocavities, which is 1.89 million and thus sufficiently high for devices. It is noted that the Q_{exp} of all three cavities on chip A8 are lower than those of the other 27 cavities, which suggests an error in our small-scale fabrication process and not a problem in the CMOS process. An unintentional oxidation or contamination of the surface probably resulted in a large extrinsic absorption loss. Therefore, we omit chip A8 from the following discussion and find that the remaining chips (with a total of 27 cavities) exhibit a similar magnitude of the fluctuation of Q_{exp}. The average Q_{exp} without the A8 chip is 1.97 million. Figure 4(b) shows the histogram of Q_{exp} for the 27 cavities, which evidences that they are uniformly distributed. Therefore, we conclude that the Q_{exp} values fabricated by the CMOS process are independent of the position on the 300-mm-wide SOI wafer. With the following theoretical analysis of the hole geometry imperfections we can understand that the magnitude of the standard deviation of the hole geometry (σ_{hole}) is almost the same in any position of the wafer, even if the average geometry shifts.

We found that the Q_{exp} values are much smaller than $Q_{ideal} = 3.31 \times 10^7$, which is attributed to the scattering loss ($1/Q_{scat}$) from random variations in the air hole geometry and from optical absorption loss ($1/Q_{abs}$) related to the surface [27-29,40-42]. The difference between Q_{exp} and Q_{ideal} can be expressed by the following relation:

$$1/Q_{exp} = 1/Q_{ideal} + 1/Q_{scat} + 1/Q_{abs} \tag{3}$$

For the present analysis we consider that $1/Q_{abs}$ is about 1.25×10^{-7} [43]. The scattering loss $1/Q_{scat}$ can be estimated with a numerical calculation. We estimated the influence of variations in the air hole radii and positions for the measured 27 nanocavities using a 3D FDTD calculation that accounts for air hole imperfections [29]. Details of the calculation method are given in [28]. Figure 5(a) shows the expected distribution of Q for nanocavities including hole geometry fluctuations (Q_{fluc}). To understand the influence of such a nonideal nanocavity geometry, thirty different variation patterns with a standard deviation of $\sigma_{hole} = 1$ nm (a random deviation of δr, δx, or δy with a magnitude of 1 nm) were used. The thirty patterns were the same as those in previous study and thus the distribution of Q_{fluc} in Fig. 5(a) is similar to the previous report [28,30]. The calculated Q_{fluc} values are much smaller than Q_{ideal} because of Q_{scat}. These three values of Q are relation via

$$1/Q_{scat} = 1/Q_{fluc} - 1/Q_{ideal} \tag{4}$$

This statistical simulation yielded the following relations for the average value of $1/Q_{scat}$, $\langle 1/Q_{scat} \rangle$, and the standard deviation of $1/Q_{scat}$, $\sigma_{1/Q scat}$, because they are proportional to the square of σ_{hole} [28, 29]:
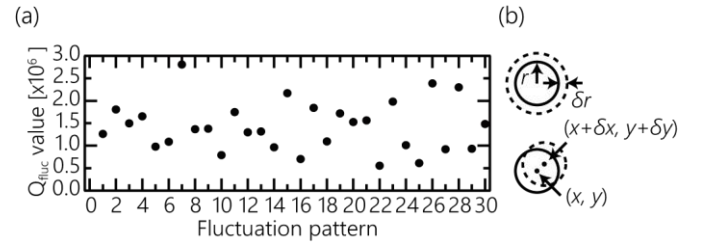

Fig. 5. (a) Calculated Q factors of nonideal nanocavities with a structure as shown in Fig. 1(b). The nonidealities were simulated by using thirty different fluctuation patterns with $\sigma_{hole} = 1$ nm. (b) Schematic view of the variation in the air hole radius and position. δx and δy represent the deviation from the ideal position. δr represents the deviation of the radius.

$$\langle 1/Q_{scat} \rangle = 7.90 \times 10^{-7} \times \sigma_{hole}^2 \tag{5}$$

$$\sigma_{1/Q scat} = 3.48 \times 10^{-7} \times \sigma_{hole}^2 \tag{6}$$

These coefficients of 7.90×10^{-7} and 3.48×10^{-7} are larger than the previous report in spite of the same variation patterns [30]. This is because the radius of the PC used in this study was larger. The larger radius increases the value of $1/Q_{scat}$ for the same magnitude of σ_{hole} because the refractive index variation induced by the air hole fluctuation is increased. The values of $\langle 1/Q_{scat} \rangle$ and $\sigma_{1/Q scat}$ for the data shown in Fig. 4 were estimated to be 3.64×10^{-7} and 7.41×10^{-8}, respectively. By using these values, (5) yields $\sigma_{hole} = 0.68$ nm and (6) yields $\sigma_{hole} = 0.46$ nm. Because both values have the same order of magnitude, we consider that the result is plausible and we use the arithmetic mean $\sigma_{hole} = 0.57$ nm in the following discussion. This value is smaller than those of our previous study, which means that the present sample structure and fabrication method provides significant improvement [30].

It is interesting to note that for the 7 chips A3, A8, D2, D5, G2, G5, and G8 the 4th cavity exhibits the highest Q_{exp} among the 4 cavities on the same chip. This suggests that the photomask for the 4th cavity has an air hole pattern that decreases $1/Q_{scat}$. In other words, the Q_{exp} values depend on the accuracy of the photomask pattern. By using a photomask with a better accuracy, the Q_{exp} can be further improved. We confirmed that the shapes of the air holes fabricated with CMOS-compatible lithography (Fig. 1(b); inset) are inferior to those fabricated with EB lithography. At present, the lowest reported value of σ_{hole} for EB fabrication was 0.25 nm which enabled a Q_{exp} of 11 million; the highest PC nanocavity Q value reported so far [13].

C. Discussion of the λ_{exp} fluctuation

Figure 6(a) shows the distribution of λ_{exp} for the thirty measured nanocavities. The solid line indicates the average value of λ_{exp}, 1574.5 nm, which is almost the same as the calculated wavelength λ_{ideal}. It is noted that for the 7 chips A3, A5, D2, D5, G2, G5, and G8 the 4th cavity has the longest λ_{exp} among the 4 cavities on the same chip. The photomask for the 4th cavity will have an air hole pattern that slightly increases the effective refractive index. A similar phenomenon was also observed for the Q_{exp} presented in Fig. 4(a) and thus we conclude that the accuracy of the photomask for each

nanocavity influences the optical properties of the ultrahigh-Q nanocavities.

The magnitude of the fluctuation of λ_{exp} within a chip is less than 2 nm, which is the same order of magnitude as that for previous studies [29, 30]. On the other hand, the average λ_{exp} obtained for each chip shows a strong variation. Among the 9 chips, the difference of the chip-averaged λ_{exp} is as large as 8.0 nm (between chip D2 and G2). The dashed lines in Fig. 6(a) indicate the standard deviation of 2.47 nm for the thirty cavities, which is about 5 times larger than that reported previously for a single chip [30]. Such a large variation is undesirable for optical link applications.

The simulation presented in Sec. 4.2 also yields the following relation for the standard deviation of λ, which is known to be proportional to σ_{hole} [28].

$$\sigma_\lambda = 0.66 \times \sigma_{hole} \tag{7}$$

By substituting the average $\sigma_{hole} = 0.57$ nm obtained from the analysis of Q_{scat}, we obtain $\sigma_\lambda = 0.38$ nm. The experimental value for the thirty cavities is much larger than this expectation value, which is in contrast to previous reports investigated for the ultrahigh-Q nanocavities fabricated within a local area (~ 1 cm^2) [29, 30]. Therefore, we consider that mechanisms other than the σ_{hole}, random air-hole geometry variations, cause the observed large variation of λ_{exp} for the nine chips in the 300-mm-wide SOI wafer.

It is noted that the simulation including the air hole variations were performed with fixed values for the average radius (113 nm), the lattice constant (410 nm), and the slab thickness (219 nm). However, some of these three values can shift depending on the position on the 300-mm-wide SOI wafer. Even if these three structural parameters shift by several nanometers, the magnitudes of Q_{exp} or $\langle 1/Q_{scat}\rangle$ will not change drastically as long as the same magnitude of σ_{hole} is maintained. On the other hand, the λ changes significantly. Therefore, the prediction made via (7) is in good agreement with the experimental results for the nanocavities fabricated within a local area only, i.e., the standard deviation of λ_{exp} within a chip can be comparable with the theoretical value.

According to the FDTD calculation, the λ for the nanocavities measured in this study should change by 3.0 nm for a 1-nm change of the lattice constant, by -2.7 nm for a 1-nm change of the radius, and by 0.67 nm for a 1-nm change of the thickness. The change of the lattice constant can occur only during the photo-lithography process while the change of the average radius (r in Fig. 5b) can occur in several processes. The variation of the slab thickness for the measured 9 chips is almost inherent to the 300-mm-wide SOI wafer.

Figure 6(b) shows the relation between the chip-averaged λ_{exp} and the chip position. The horizontal plane represents the chip position. The λ_{exp} for the chips of D2, D5, and D8 are longer than those for the other chips. The positions of measured nanocavities for these three chips are closer to the center of the substrate than those for the other chips as shown in Fig. 1(e). Therefore, this graph indicates that λ_{exp} tends to shift to shorter wavelengths as the chip gets closer to the substrate edge. Figure
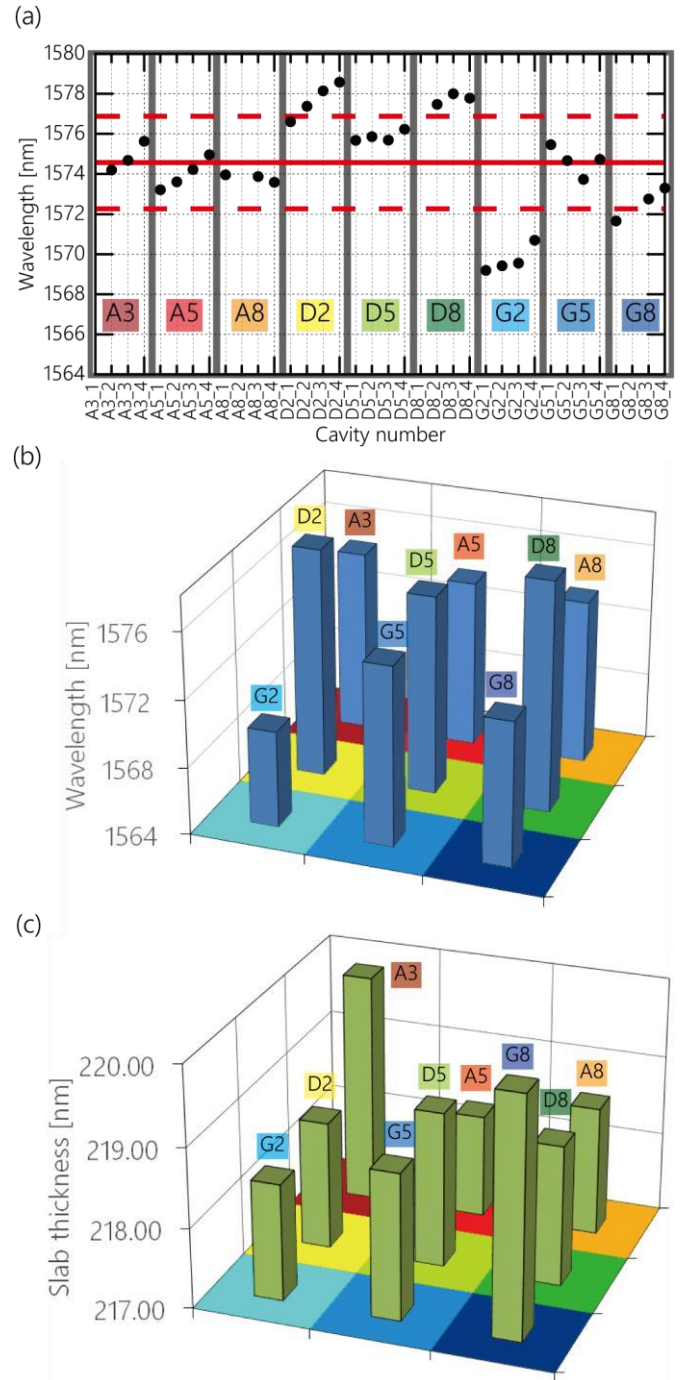

Fig. 6. (a) The experimental λ of the measured nanocavities. The red solid line represents the average λ for all thirty cavities. The dashed lines indicate the σ_λ of 2.47 nm. (b) Relation between chip position and chip-averaged λ for the nine chips. (c) Relation between chip position and chip-averaged slab thicknesses for the nine chips.

6(c) shows the thickness of the slab for the 9 chips, measured by spectrally-microscopic reflectometry (Otsuka Electronics FE-3000). The measurement accuracy is about 0.1 nm. The height of the bars indicates the surface slab thickness and the horizontal plane shows the chip positions. Among the 9 chips, the maximum difference of the slab thickness (between chip G8 and A5) is only 2.4 nm, which is too small to explain the difference of 8 nm in chip-averaged λ_{exp}. In addition, the chip A3 has the largest slab thickness among the 9 chips while the

TABLE II
AIR HOLE RADII FOR SEVERAL CHIPS MEASURED BY THE SEM

Chip	Radius (nm)	Chip	Radius (nm)
A6	116.2	E6	113.4
B6	114.0	E7	116.6
C6	114.7	E8	115.5
D6	114.9	E9	117.0
		E10	118.6

Measured chips are indicated in Fig. 1(e).

chip-averaged λ_{exp} of A3 shown in Fig. 6(b) does not have the longest λ_{exp}. Similarly, for other chips, there is no strong correlation between the slab thickness and the chip-averaged λ_{exp}. The shift of the slab thickness is not the main cause for large chip dependence of λ_{exp}.

The photolithography process could cause a shift of the radius or the lattice constant. In order to draw the lithography pattern for the 60 chips, it is necessary to move the wafer stage of the stepper. If the stage height deviates from the focal point for the photolithography, the projected radius and the lattice constant increase. When the air hole radius becomes larger, the λ shifts to a shorter wavelength. On the other hand, when the lattice constant becomes larger, the λ shifts to a longer wavelength. Therefore, the wavelength shift induced by the deviation of the stage height should cancel to a certain degree. To induce a change in λ_{exp} of more than 8 nm, the stage height has to move largely, which would also significantly increase the magnitude of σ_{hole} for the nine chips. However, there is no correlation between the fluctuation of the chip-averaged λ_{exp} and the fluctuation of Q_{exp} (Fig. 4). Therefore, we consider that the photolithography process is not the main cause for the λ_{exp} fluctuation.

From the above we infer that a systematic change of the average air hole radius should be the main cause for the large position dependence of λ_{exp}. The change of the average air hole radius can occur in various processes such as the exposure of the resist pattern, the plasma etching, and the cleaning process. In all these cases, the process conditions are optimized for the center of the 300-mm-wide SOI wafer. Therefore, the average air hole radius tends to change as its location moves from the center of the wafer towards the edge. Figure 6 (b) shows that the λ_{exp} of the nanocavities located far from the center of the wafer shift to a shorter wavelength. Thus, the average air hole radius is expected to be increased by several nanometers at the edges of the wafer. Table II presents the air hole radii for several chips analyzed by the SEM, A6 ~ D6 and E6 ~ E10, which continuously distribute from the center of the wafer to the edge (9 pieces used for the spectral measurement were undesirable for the SEM analysis since they were bonded to cubic blocks with a nonconductive adhesive). The accuracy of the SEM (JEOL JSM-7610F) was about 2 nm. Measured radii showed a tendency that we expected. We conclude that the shift of the average radius is the main cause for large wafer position dependence of λ_{exp}. The main procedure inducing the systematic shift of the radius should be identified in future (we suspect the plasma etching) [44]. It is noted that the change for

the tilt of the air holes also induces the change of the average radius. The decrease of average tilt from 2.5 to 2.0 degrees corresponds to an increase of the average radius of 1.0 nm. Improvement of CMOS process should be performed taking the change of the average tilt of air holes into consideration.

V. SUMMARY

We measured the Q_{exp} and λ_{exp} of thirty ultrahigh-Q heterostructure nanocavities distributed over nine chips at various positions of a 300-mm-wide SOI wafer. The nanocavities were fabricated using a CMOS process with 193-nm ArF immersion photolithography where the design of the nanocavity and the fabrication process were improved to increase the Q_{exp}. The Q_{exp} values were independent of the position on the 300-mm-wide SOI wafer. The average Q_{exp} value was 1.9 million, which is sufficiently high for applications, and the highest value of 2.5 million was obtained. On the other hand, the chip-averaged λ_{exp} were strongly dependent on the position. They tended to shift to shorter wavelengths as the distance between the measured chip and the substrate center increased. We concluded that the main cause is a change in the chip-averaged radius by several nanometers. In order to further increase the Q_{exp} and to decrease the variation of the chip-averaged λ_{exp}, the improvements of the photomask, the SOI wafer, and the CMOS process is important. The CMOS process should be improved so that the random variations of air holes in a local area and the overall shift in the average radius in a 300-mm-wide SOI wafer are reduced with the high reproducibility. Studies on such optimization of the CMOS process will accelerate the application of the PC nanocavities. This will enable the mass production of various exotic devices based on the ultrahigh-Q nanocavities including ultralow threshold Raman Si lasers [19].

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