Multi-Mode Oscillators Using BBD

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The oscillator using delay element in its feedback path has been well known. Its feature is that the oscillating frequency is determined by the delay time. As a result, several applications are possible.

In this paper, the oscillator using BBD as a delay element is described aiming the exactness, the compactness and the stability. On the basis of this oscillator, the multi-mode oscillator with many oscillating frequency, can be easily obtained.

Some applications such as the frequency memory and the non-linear down converter are also described.

1. Introduction

The multi-mode oscillators paying attention in its feedback path have been well known. They are as following;

[1] the asynchronous multi-mode oscillator[1] has some parallel tank circuit connected with some switches in feedback path,

[2] the asynchronous multi-mode oscillator has the transmission line type delay elements instead of the previously parallel tank circuits,

[3] the multi-mode oscillator[2] with the frequency memory function has some tank circuits connected in parallel or series and is with the trigger terminal for forced sinusoidal input by each suitable amplitude values,

[4] an overtone type multi-mode oscillator has been realized by using the crystal[3], where the over-tone means to stand some integer number's waves on the crystal. Such integer number's frequency corresponds to the multi-mode oscillating frequency. As a result, the abilities of all the crystal oscillator have been characterized by their stability and exactness of crystal.

The conventional oscillators mentioned above have some defects. The asynchronous one is too primitives. The transmission line type one is bulky. The frequency memory type one is aged and complicated in the structure. The multi-mode oscillator replaced by crystal is compactness, but is very sensitive with surrounding temperature and with crystal's cutting.

On the other hand, recently, BBD (bucket brigade device) as a charge coupled IC device, has been developed. Since this is a kind of a multi-stages delay circuit, all the organization are controlled by the external clock signal.

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Then, in order to obtain more exact and stable multi-mode oscillator, the introduction of BBD is proposed in stead of the crystal or the delay elements. In this case, since the delay time is severely controlled by the external clock signal source, the oscillating frequency can be adjusted continuously.

Furthermore, by replacing the single constant clock source to some clock sources including any variety functions, the non-linear converter and the frequency memory are possible.

Most important point for the exact and the stable operations are that the proposed oscillator is not used as a single circuit, but can be used as an oscillator in the modern sampled data system or the digital system. The reason is that the clock signal has been severely controlled from external source.

In this paper, the operational principle, the relation between the oscillating frequency and the clock one and a multi-mode operations are explained first. Next, the experimental results are described according to the principle. Last, the applications to the down converter and to the frequency memory are shown with the tentatively experimental results.

2. Operational Principle

An oscillator using general delay element as shown in Fig. 1 is discussed first. The oscillating conditions in Fig. 1 are as following I and II . That is

I Loop gain is unity,

II Positive feedbakc loop exists.

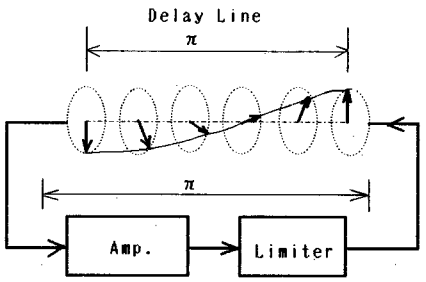

Fig. 1 Principle of Oscillator using General Delay Element.

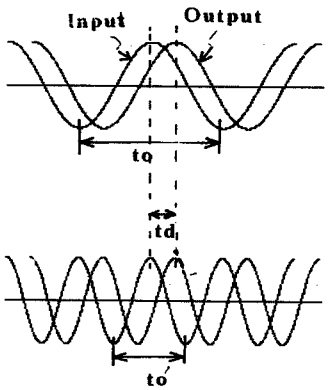

Fig. 2 Change of Input and Output Voltages at Delay Circuit with Time.

I is satisfied, because the amplitude limiting circuit using thermister has the voltage gain. II is also enough, because the electric circuit has the phase difference π radian, and because the phase of voltage of output terminal in the delay element has the lagging phase difference of π radian with that of input terminal.

Figure 2 shows the changes of input and output voltages at delay circuit with time in case of the lower frequency and the higher frequency. The time delay of the delay circuit, t_d, is the same in both case, whereas the lagging phase ϕ changes with the different period t_0 described in Eq. (1)

$$\phi = 2\pi \frac{t_d}{t_0} \tag{1}$$

Equation (1) means also that if ϕ is (1 + 2P) π, (P = 0, 1, 2. ·····), this circuit oscillates.

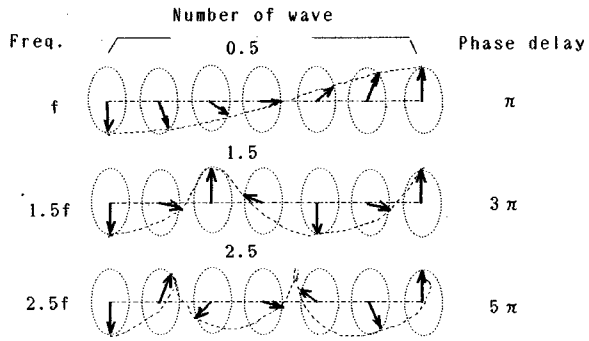

Fig. 3 Vector Rotation on Delay Circuit.

Figure 3 shows the voltage vector rotation on the delay circuit in case of different frequencies under the condition that the phase difference ϕ satisfies the oscillating condition. This corresponds to the over tones type oscillation in the crystal. In this figure, the phase difference ϕ is π only. Of course, this theory can be applied to the case of 3π, 5π, ·····, described in following Eq. (2).

$$\phi = (1 + 2P)\,\pi \tag{2}$$
$$P = 0, 1, 2, \cdots\cdots$$

As a result, the frequency f_0 of this circuit is described in Eq. (3).

$$f_0 = \frac{(1 + 2P)}{2t_d} \tag{3}$$

where oscillating frequency f_0 is $1/t_0$.

In the Fig. 1, if the phase differences of the amplifier's and limiting circuit are 0, 2π, 3π, ·····. and if the phase differences of the delay line circuit ϕ are $2(1+P)\pi$, (P = 0, 1, 2, ·····), this circuit oscillates. As a result, the oscillating condition ϕ is rewritten as follows,

$$\phi = 2\pi \frac{t_d}{t_0} = 2\,(1 + 2P)\pi \tag{4}$$

and the oscillating frequency f_0 is determined as following Eq. (5).

$$f_0 = \frac{(1 + P)}{t_d} \tag{5}$$

Equation (3) means this circuit oscillates when the number of wave on the delay circuit is multiplied 0.5 by the odd integer numbers as shown in Fig. 3, whereas in case of Eq. (5), the number of wave is multiplied 0.5 by the even integer numbers.

Next, if the delay element is BBD, its delay time changes with the clock signal frequency f_c described in following Eq. (6).

$$t_d = \frac{N}{2f_c} \tag{6}$$

where, N is the number of stage of BBD.

Substituting Eq. (6) to Eq. (3), the oscillating frequency f_0 is

$$f_0 = \frac{(1 + 2P)}{N} f_c \tag{7}$$

That is, the oscillating frequency f_0 is proportional to the clock frequency f_c.

3. Experimental Results

Figure 4 is the experimental circuit using BBD (N = 1024 stages). Their experimental results are shown in Fig. 5. In the experiments, the phase difference appeared on the three-stage operational-amplifiers in 3π radians. As a result, it can be seen from Eq.(2) that the oscillation occurs when the phase difference in BBD are π, 3π, 5π, ... radians. This corresponds to P = 0, 1, 2, ... In this case, the oscillating frequency f_0 moves with changing the clock frequency f_c in the left or right direction on the gothic line in Fig. 5.

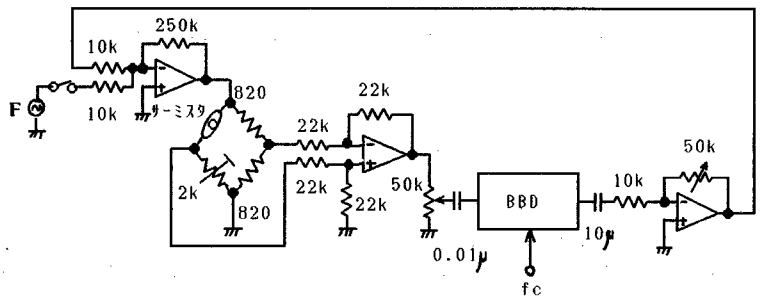

Fig. 4 Experimental Circuit.

4. Application

From the oscillator as shown in Fig. (4) and from the characteristics of Fig. 5, the applications to the frequency memory and to the down converter with sinusoidal output are considered.

4.1. Frequency memory

This is the same idea with the conventional paper 1). However, the advantage in this method is that the memory frequency is freely able to change with the clock frequency. Figure 6 shows the illustration of Eq. (7) as same with Fig. 5. If the specified clock frequency f_{CO} is given as shown in Fig. 6, the oscillating condition written in Eq. (7) is satisfied. Its oscillating condition is shown at - mark in Fig. 6.

If the oscillation occurs at point X of the △ mark, and if the trigger frequency F from the external source is applied to the trigger terminal as same with the circuit of Fig. 4, the oscillating frequency shifts to point Y in which frequency is most close to the frequency F. This phenomenon means the operation of frequency memory as shown in Fig. 6. The memory frequency moves with changing the clock frequency f_c.

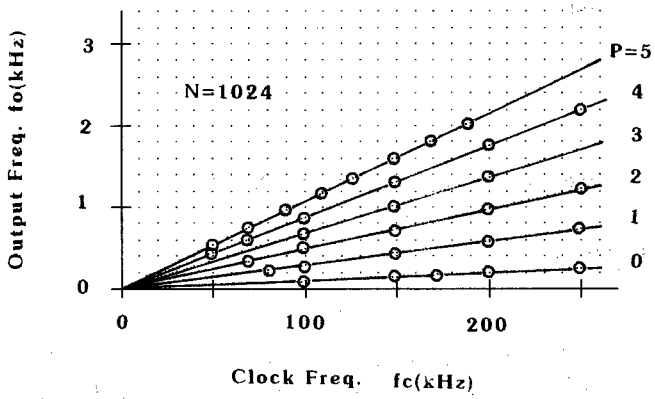

Fig. 5 Experimental Results of Figure 4.

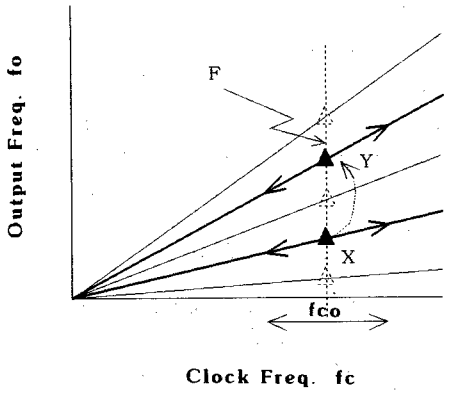

Fig. 6 Operation of Frequency Memory.

4.2. Non-Linear type Down-Converter with Sinusoidal Output

As mentioned in 4.1, the sinusoidal output of the proposed multi-mode oscillator can be obtained by dividing the clock frequency f_c. This is a big feature, since the output of the frequency divided in digital technology is rectangular wave.

Furthermore, by using BBD with the constant delay time (f_s; constant) as shown in Fig. 7, the non-linear type down-converter with the sinusoidal output can be realized.

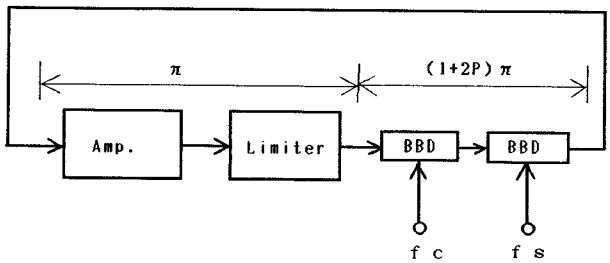

Fig. 7 Block Diagram of Non-linear Type Down Converter.

If the delay time of BBD controlled by the clock frequency f_c in Fig. 7 is t_s, the following Eq. (8) is obtained,

$$t_s = \frac{N_2}{2f_s} \tag{8}$$

The total delay time, $t_d + t_s$, of two BBDs in Fig. 7 is

$$t_d + t_s = \frac{N_1 f_s + N_2 f_c}{2 f_s f_c} \tag{9}$$

where, N_1 and N_2 are the numbers of stages of the respective BBDs. As a result, from Eq. (3) the oscillating frequency of this circuit is given as following Eq. (10),

$$f_0 = \frac{(1 + 2P) f_s f_c}{N_1 f_s + N_2 f_c} \tag{10}$$

where, if f_s is constant, the relation between the oscillating frequency f_0 and the clock frequency f_0 is the non-linear.

Figure 8 is the simulation results of non-linear type down converter. Figure 8 also explains well the Eq. (10) under the conditions, $N_1 = N_2 = 512$, the clock frequency f_s; 100 kHz, 200 kHz and 400 kHz.

5. Conclusion

As mentioned above, a newly multi-mode oscillator using BBD was proposed. This has been improved from the conventional oscillator paying attention in its feedback path. This means the replacing from the LC tank circuits, transmission line type delay line and a crystal to BBD.

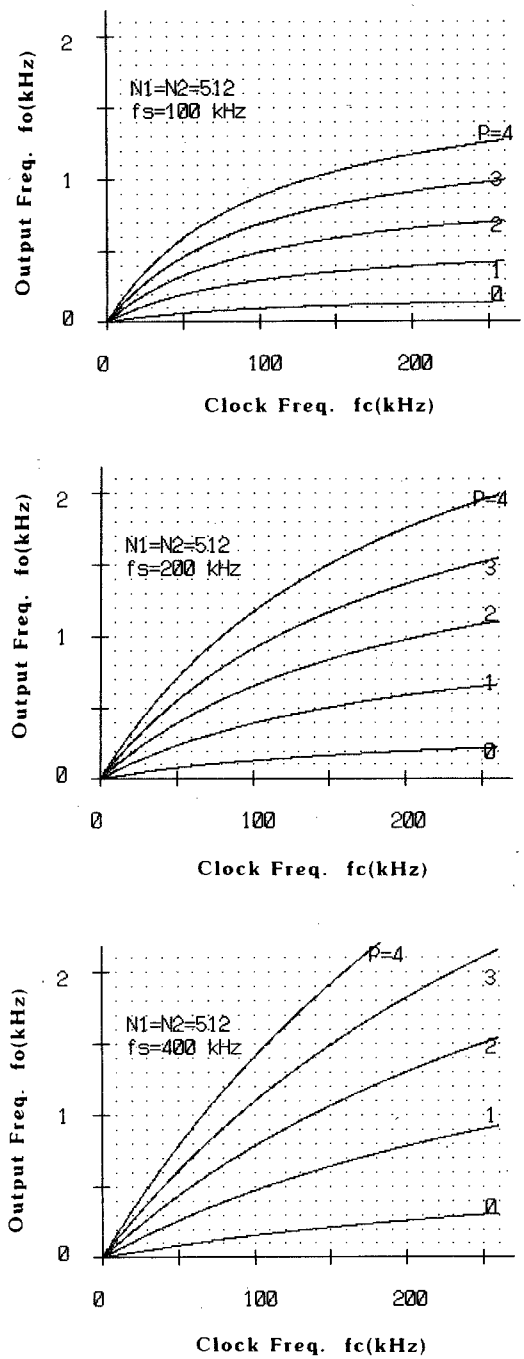

Fig. 8 Simulated Results of Down Converter.
(a) f_S = 100 kHz. (b) f_S = 200 kHz. (c) f_S = 400 kHz.

As a result, the proposed oscillator has some features, the exactness, the compactness and the stability because BBD is controlled by externally and severely mastered clock signal.

Furthermore, by fine controlling the clock signal, and by combining BBD with the different kinds of characteristics, lots of applications are possible. In this paper, two application of them, the frequency memory and the non-linear type down converter were described.

References

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