Switched Capacitor Amplifiers

Switched Capacitor Amplifiers

Yoichi JYO*, Kazuya IWATA**, Suemitsu MINAMOTO*, and Yoshiaki KOJIMA*

(Received June 15, 1985)

The approach to synthesis taken in this paper will be to configure the two-phase clock switched capacitor (SC) amplifiers to simulate the conventional continuous time RC amplifiers as much as practicable.

Advantages of this approach are;

1) We can design the SC amplifiers by using classical continuous time theory directly.
2) We can reduce the circuit complexity as we assume a two-phase clock.

Several circuits are designed, built with the discrete components, and tested. Theoretical results are compared to experimental ones.

1. Introduction

Switched capacitor (SC) networks have been recongnized as an efficient tool for performing analog signal processing in the form of monolithic integrated circuit. This is due to the recent availavility of suitable MOS operational amplifiers, as well as high quality MOS capacitors and switches. The physical size of all components can be made sufficiently small. The integrated resistors have poor temperature and linearity characteristics as well as requiring a large amount of silicon area. The concept of switched capacitors was originally introduced to replace resistors in the implementation of active MOS integrated filters. Resulting filters have characteristics that depend only on ratios of capacitances, with a frequency scale proportional to the frequency of a clock. The *switched capacitor resistors* require very little silicon area to implement large resistance values. In fact the silicon area decreases as the required value of resistance increases.

Such an appealing feature is a good motivation for investigating new application areas beyond the traditional simulation of analog filters.

Recently Seki et al. developed several circuit realizations for SC amplifiers by replacing the resistors of the conventional RC amplifiers by equivalent switched capacitors[1),2)]. The SC amplifier has the advantages that various characteristics can be controlled by the clock frequency and it achieves very low power consumption because active elements act during only the charge transfer period. Seki's circuits require a three-phase clock signal rather than the usual two-phase one, then the situation is more complicated due to the elavorate clocking scheme.

It seems interesting to research for more advantageous circuit realizations.

This paper describes the principle for the realization of a SC amplifier especially designed to operate by a two-phase nonoverlapping clock.

The frequency characteristics of SC amplifier are the function of the clock frequency f_c and the maximum frequency of input signal to the SC amplifier is restricted by the frequency derived from the sampling theorem. Thus, the higher the frequency is, the wider the frequency region where the faithful amplifying operation is performed

* Department of Electronics, College of Engineering
** Graduate Student, Department of Electronics, College of Engineering

becomes. Therefore, the clock frequency should be chosen as high as possible. From the standpoint of constructing circuits, the frequency of a two-phase clock signal, which is higher than that of a three-phase clock one, can be easily obtained. Then it is expected that a two-phase clock SC amplifier allows higher frequency amplifying operations than a three-phase clock one. And it is possible to reduction of the whole circuit scale because the digital controlling logic becomes very simple.

2. Switched Capacitor "resistors"

In many exciting designs, the switched capacitor is grounded and switched between the nodes, as shown in Fig. 1 (a). A switch is assumed to be an element with zero impedance in the closed position and infinite impedance in the open position. A clock is a sequence of nonoverlapping pulses used for operating the switches. A two-phase clock as shown in Fig. 1 (c) is assumed. In Fig. 1, as in all other circuits, a switch will be represented with the symbols ϕ_1 or ϕ_2. The symbols ϕ_1 and ϕ_2 will indicate the phase of the clock during the switch is closed. In Fig. 1 (a), the switch is in the left hand position during the clock phase ϕ_1 and in the right hand position during the phase ϕ_2.

It can be easily shown that the average current i_2 delivered by the capacitor to node *2* is $(C/T_c)\,[v_1 - v_2]$ where T_c $(= 1/f_c)$ is the switching (clock) period and f_c should be large compared to the maximum frequency of interest. Thus in this restricted sense, the circuit of Fig. 1 (a) is equivalent to a conductance C/T_c connected between nodes *1* and *2*. An alternative circuit, which operates by charging and discharging C is shown in Fig. 1 (b).

Using the circuits of Fig. 1 as basic building blocks, it is possible to design SC amplifier.

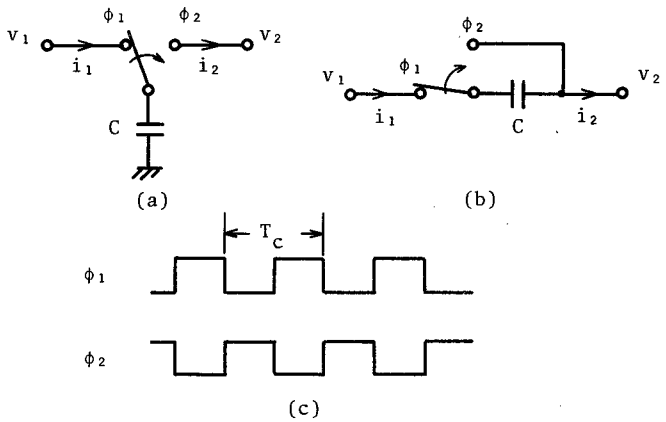

Fig. 1 Switched capacitor equivalents of a resistor.
(a) Shunt capacitor. (b) Series capacitor.
(c) Timing diagram.

3. SC Amplifiers

A conventional self bias FET amplifier using resistors is shown in Fig. 2 (a). Each resistor is replaced by a switched capacitor arrangement on a one-to-one basis. The resultant SC amplifier which is made up of FET and four capacitors C_g, C_s, C_d, and C_{sa}

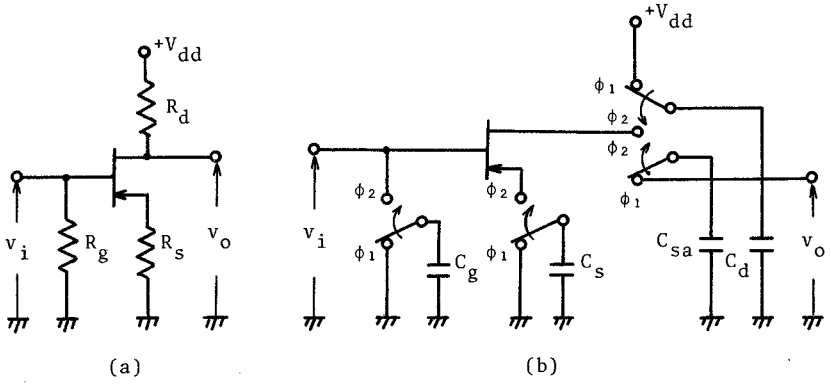

Fig. 2 Self bias amplifier.
(a) Conventional amplifier.
(b) Switched capacitor version of (a).

switched at the clock frequency f_c is shown in Fig. 2 (b).

An important difference between Seki's SC amplifier and the circuit of Fig. 2 (b) is that C_{sa} is added to the circuit to sample and hold the output signal v_o. And all switches are controlled by a two-phase clock.

The following equations should hold.

$$C_g = 1/(R_g f_c) \tag{1}$$

$$C_s = 1/(R_s f_c) \tag{2}$$

$$C_d + C_{sa} = 1/(R_d f_c) \tag{3}$$

By choosing capacitors whose values are designed from Eqs. (1) ~ (3), the equivalent self bias SC amplifier can be obtained.

The outline of the circuit operation is as follows. The gate resistor R_g is replaced by switched capacitor C_g. The capacitor C_s is connected to the source of FET during the phase ϕ_2. During the phase ϕ_1 the charge of the capacitor C_s is removed by short circuiting it. The capacitor C_d is charged to the power supply voltage $^+V_{dd}$ in phase ϕ_1 and switched to the drain of FET in phase ϕ_2. Therefore, FET operates during only the clock phase ϕ_2. The capacitor C_{sa} is charged to the output voltage v_o in phase ϕ_2 and then holds it until the next sampling period.

Fig. 3 (a) shows an alternative amplifier using resistors and Fig. 3 (b) shows an equivalent SC amplifier. The load circuit is constructed in the same way as the circuit of Fig. 2 (b). The biasing circuit is made up of three capacitors C_1, C_2, and C_3 switched at the clock frequency f_c. During the phase ϕ_2, the capacitors C_1 and C_2 are connected in a series and the new voltage V_1 at the a-node becomes V_g. During the phase ϕ_1, C_2 is grounded and S_1 is closed, then V_1 equals V_{dd}. The b-node voltage V_2 equals zero in phase ϕ_1 and V_g in phase ϕ_2. The input signal superposed upon the bias voltage V_g is applied to the gate of FET by the combination of C_3, S_3 and S_4. Fig. 4 shows the timing example of the biasing circuit.

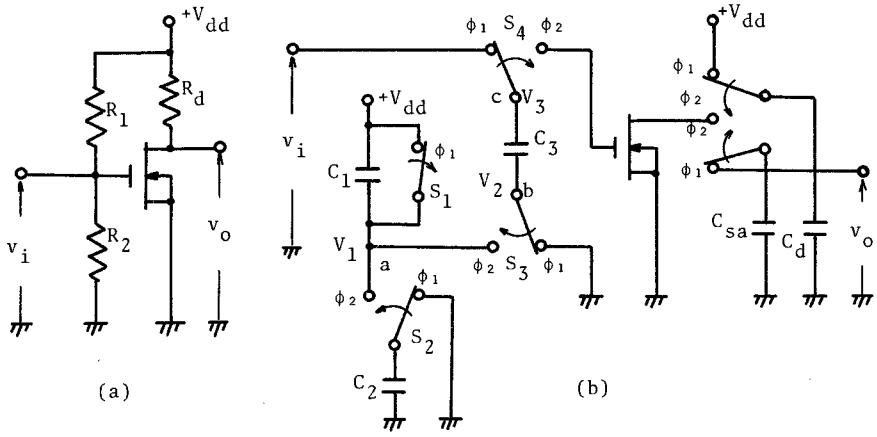

Fig. 3 (a) Alternative self bias amplifier.
(b) Switched capacitor version of (a).

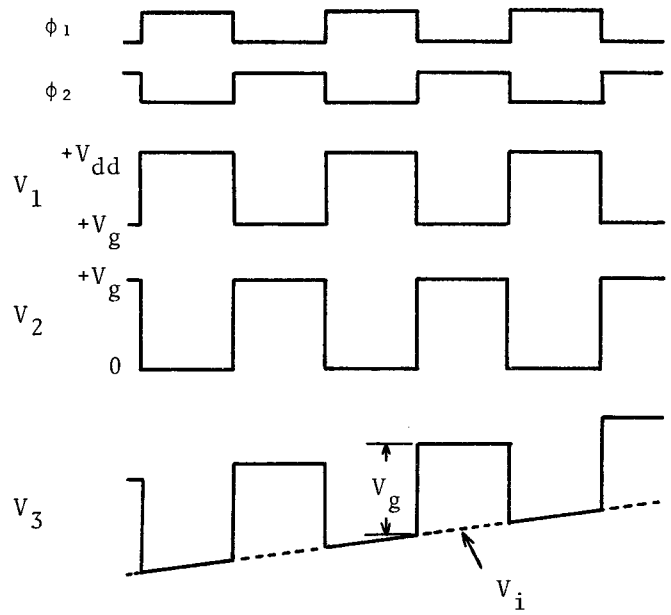

Fig. 4 Timing example of the biasing circuit.

The bias voltage V_g is determined as follows.

$$V_g = \frac{C_1}{C_1 + C_2} V_{dd} \tag{4}$$

Then the following relation can be obtained.

$$C_1/C_2 = R_2/R_1 \tag{5}$$

We will mention briefly about the relation between the gain and the clock frequency f_c. The voltage gain A_v of FET amplifier can be obtained as

$$|A_v| \fallingdotseq g_m R_d \tag{6}$$

where g_m and R_d are the transconductance of FET and the load resistance respectively.

Substituting Eq. (3) to Eq. (6),

$$|A_v| = \frac{g_m}{(C_d + C_{sa}) f_c}. \tag{7}$$

Then,

$$20 \log|A_v| = 20 \log\left\{g_m/(C_d + C_{sa})\right\} - 20 \log f_c. \tag{8}$$

From the above equation it is seen that a linear relationship is established between the gain $|A_v|$ [*dB*] and $\log f_c$.

4. Experimental Results

The circuits of Fig. 2 (b), Fig. 3 (b), and a two-stage SC amplifier are designed, built and tested.

Prior to building the SC amplifier of Fig. 2 (b), we design the conventional amplifier of Fig. 2 (a). To have the voltage gain $A_v = 13.5\ dB$, the element values are determined by the well known classical continuous time theory as follows; $R_g = 250\ k\Omega, R_s = 200\Omega$, $R_d = 3.68\ k\Omega$, where $V_{dd} = +15\ V$ and $g_m = 1.7\ mS$.

Then, substitution in Eqs. (1) ~ (3) yields the element values of the SC amplifier of Fig. 2 (b) as $C_g = 40\ pF$, $C_s = 50\ nF$, and $C_d + C_{sa} = 2.7\ nF$, when $f_c = 100\ kHz$. When we actually build the circuit of Fig. 2 (b), the modified values of capacitors given in Table 1 are used.

Table 1 Values of capacitors for the circuit of Fig. 2 (b).

C_g	41.06 [pF]	C_s	53.03 [nF]
C_d	2.247 [nF]	C_{sa}	467.0 [pF]

The circuit of Fig. 2 (b) was built using 2SK30A for FET, and HI5051 units for the switches. The calculated and measured frequency responses are compared in Fig. 5, where $f_c = 100\ kHz$. This amplifier has a region where the gain is essentially constant and in this region there is an excellent agreement between the calculated and measured curves. However, high-frequency-response curves fall off. In this experiment the *smoothing* capacitor C_h ($= 462\ pF$) is added between the output terminal and the ground. It operates as a low pass filter to reject the undesired frequency components appeared in the output signal by switching operations. A principal cause of the loss in gain at high frequencies is due to the impedance reduction of C_h according to the frequency increasing of input signal. Moreover, switched capacitors don't act like ideal resistors, because the condition that f_c must be large compared to the maximum fre-

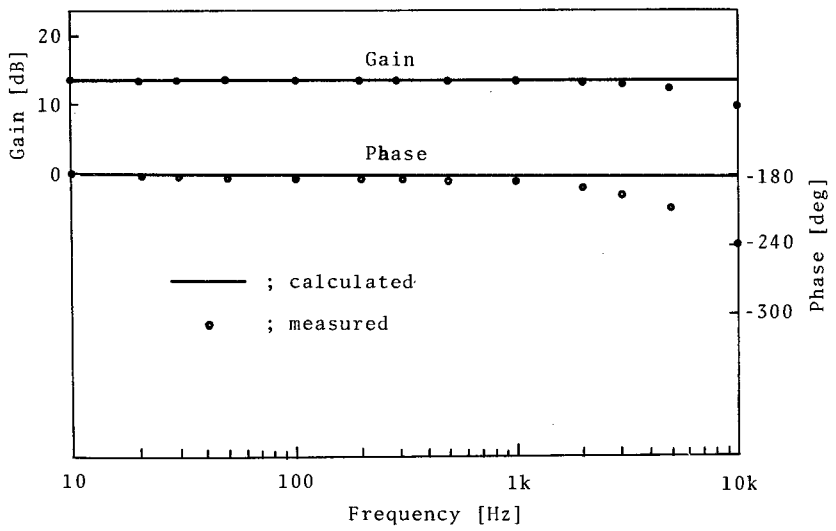

Fig. 5 Frequency responses of the circuit of Fig. 2 (b).

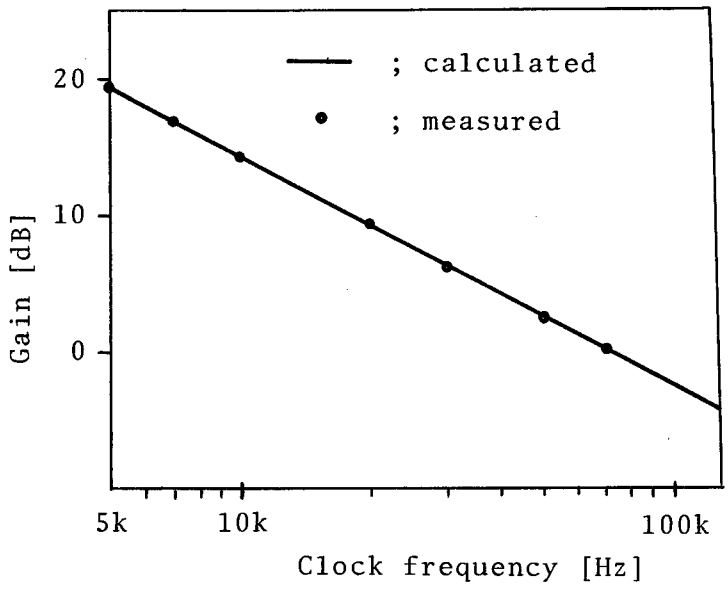

Fig. 6 A plot of gain versus clock frequency.

quency of input signal is disturbed. Then the gain falls off at high frequency region.

A plot of gain versus clock frequency is given in Fig. 6, where the input signal frequency is *100 Hz*. For this experiment capacitor values are changed so that the voltage gain is *13.5 dB* at $f_c = 10$ *kHz*. The renewed capacitor values are $C_g = 228$ *pF*, $C_s = 304$ *nF*, $C_d = 21.8$ *nF*, $C_{sa} = 2.33$ *nF*, and $C_h = 2.15$ *nF*. As f_c increases, the gain decreases straightly as mentioned in Chap. 3.

Next we show the experimental results of the circuit shown in Fig. 3 (b). The SC amplifier is designed to have the voltage gain $A_v = 18.4$ *dB* at $f_c = 15$ *kHz* and g_m of 3SK22 is *2.8 mS*. Values of capacitors are given in Table 2.

Table 2 Values of capacitors for the circuit of Fig. 3 (b).

C_1	120.0 [pF]	C_d	21.06 [nF]
C_2	3.340 [nF]	C_{sa}	1.115 [nF]
C_3	592.0 [pF]		

The calculated and measured frequency responses in the case of $f_c = 15$ *kHz* are shown in Fig. 7. To compare with the data at $f_c = 15$ *kHz*, the frequency responses at $f_c = 30$ *kHz* are shown in Fig. 7, too.

From Fig. 7 it is seen that the frequency characteristics are improved when the clock frequency f_c is high. In the high frequency region, the gain falls off by similar

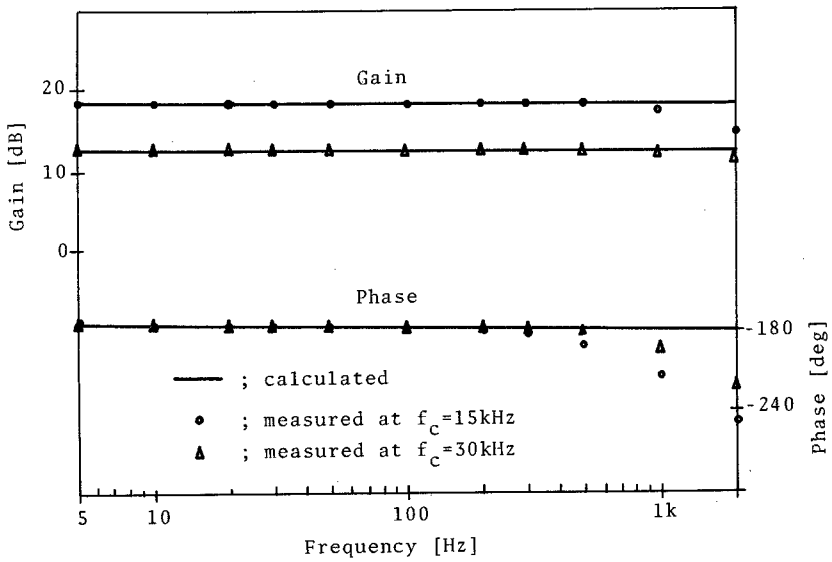

Fig. 7 Frequency responses of the circuit of Fig. 3 (b).

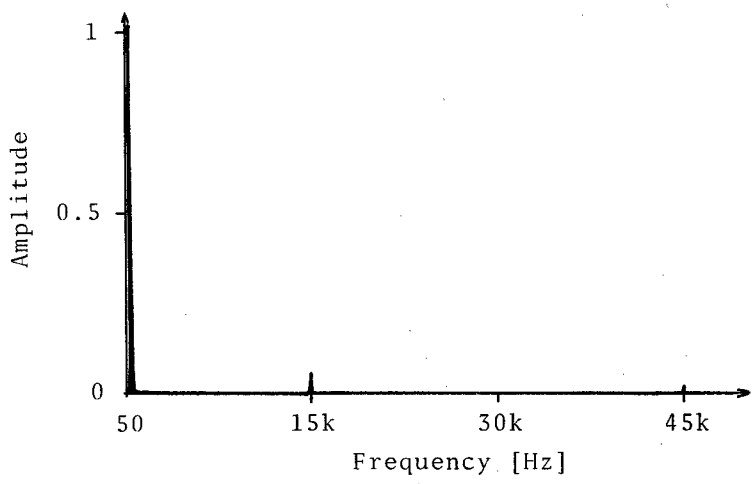

Fig. 8 Spectrum of output signal. f_c = 15 kHz, f_i = 50 Hz.

reasoning mentioned above.

In Fig. 8, we have drawn the spectrum of the output signal for $f_i = 50\ Hz$, where f_i is the input signal frequency, and $f_c = 15\ kHz$. The harmonics of clock frequency appear very slightly, therefore, the waveform distortion is very low.

Finally the two-stage SC amplifier by cascading the circuit of Fig. 3 (b) without coupling capacitor is shown in Fig. 9. Values of capacitors are given in Table 3. For FET 3SK38A is used. For the biasing circuit of second stage the negative power supply voltage $-V_{dd}$ is required to correct the bias voltage, because the output signal of the first stage contains excessive positive DC component. It is designed that the gain of the first and second stages are *10.5 dB* and *13.0 dB* respectively and $f_c = 100\ kHz$. The gain of two-stage amplifier is the product of the gains of its individual stages. The frequency

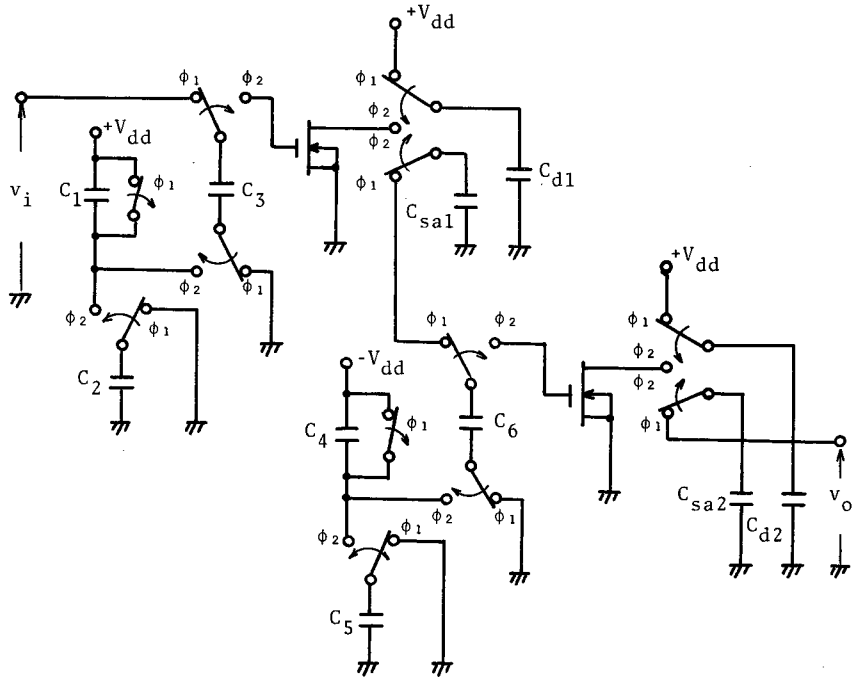

Fig. 9 Two-stage SC amplifier.

Table 3 Values of capacitors for the circuit of Fig. 9.

C_1	985.1 [pF]	C_4	9.921 [pF]
C_2	2.828 [nF]	C_5	1.274 [nF]
C_3	2.208 [nF]	C_6	425.2 [pF]
C_{d1}	1.811 [nF]	C_{d2}	2.106 [nF]
C_{sa1}	430.5 [pF]	C_{sa2}	429.8 [pF]

responses are shown in Fig. 10. Almost the expected results are obtained.

Photographs 1 and 2 show the input-output waveforms for sine and triangular inputs, where the frequency of input signal is *100 Hz*. It is appear that the waveform distortion is very low.

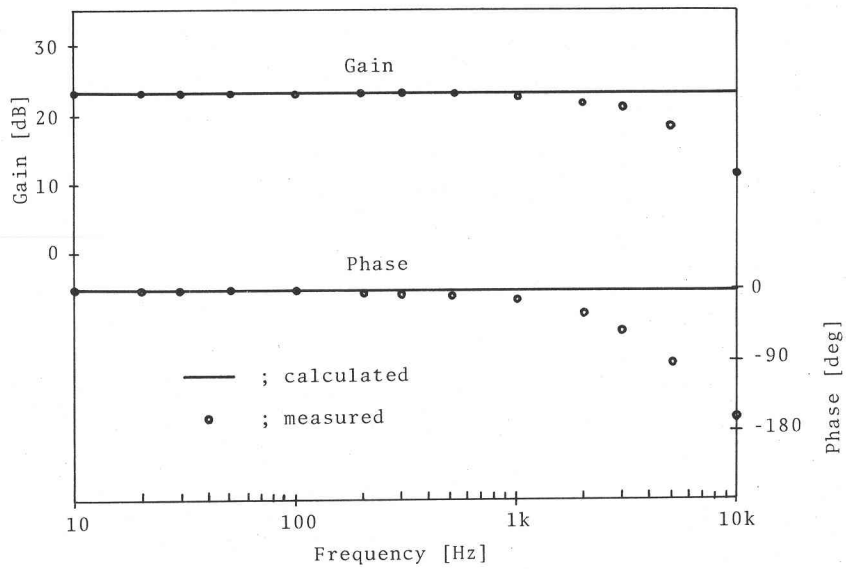

Fig. 10 Frequency responses of the two-stage SC amplifier. f_c = 100 kHz.

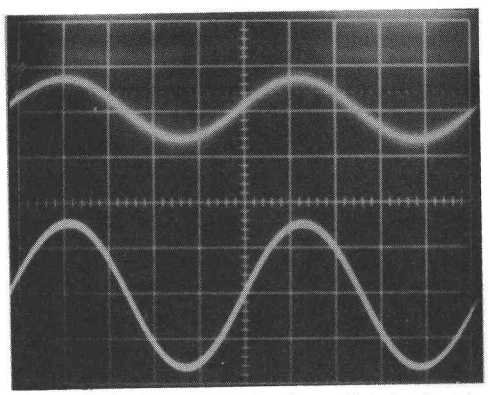

Photo. 1 Input-output waveforms for sine input signal of 100 Hz.
upper trace; input signal 500 mV/div.
lower trace; output signal 2 V/div.
f_c = 100 kHz

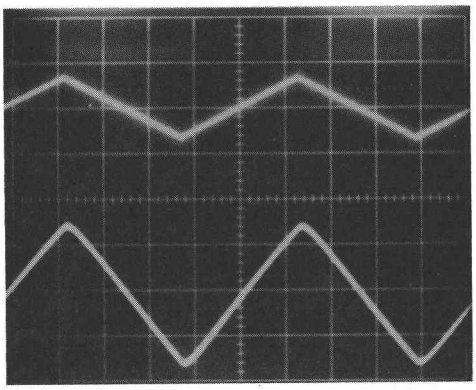

Photo. 2 Input-output waveforms for triangular input signal of 100 Hz.
upper trace; input signal 500 mV/div.
lower trace; output signal 2 V/div.
f_c = 100 kHz

5. Conclusions

In this paper, we proposed two-phase clock SC amplifiers. Some configurations of the circuit have been built and tested, and the results confirm the theoretical predictions.

The design technique is very simple and its procedure is as follows. Design the conventional RC amplifier satisfying the required specifications. Then replace the resistors of resultant circuit by the switched capacitors.

The major advantages of this circuit are;

1. Precision monolithic amplifier can be efficiently realized and its physical size can be made sufficiently small.
2. The very low power consumption can be achieved as FET operates during only the

charge transfer period.

3. The voltage gain can be controlled by the frequency of a clock.
   Therefore this approach might be applicable to many other organizations.

References

1) H. Seki, M. Yamamoto, Y. Horio and S. Mori, Trans. IECE Japan, **J 65-A**, 1196 (1982).
2) H. Seki, M. Yamamoto and S. Mori, Trans. IECE Japan, **J 67-A**, 674 (1984).