Digital Comparator

Digital Comparator

Hideo Kosako*, Katsuya Oshima* and Yoshiaki Kojima*

A problem in comparating two bit-patterns is important to screening and other functions in nearly all data-processing systems.

While the number and arrangement of components used exceed the demands for the functional requirments. Here we introduce a simple digital comparator which exhibites the functions of the high speed operation. This paper proposes principally the theoretical approaches and the experiments for the new comparator circuit.

1. Introduction

A standard method of performing a digital comparison is to use an exclusive-OR circuit for each pair of bits to be compared in two bit-patterns. Each decision of "greater than", "less than" or "equal to" is scanned serially from the most significant bits down to the least significant bits. Another approach consists of taking the complement of one register, adding it to another register and looking for the carry generated by the most significant bit. There are also some different digital comparators using many components[1].

The disadvantage for each of these methods of digital comparison is in the amount of time involved in obtaining the decision. This time loss may lie in either the scanning rate or the carry propagation time. Another disadvantage common to such method is the complex circuitry required.

A comparator that avoids these problems is discribed in this paper. This comparator obtains the decision by the voltage polarities, positive, zero and negative, generated by the most significant bit as the output of the comparator.

2. Principles

The block diagram of a comparator is shown in Fig. 1. This diagram will be used for the explanations of the comparison method to two bit-patterns of n bits.

D_0, D_1, D_2, $\cdots$, D_n denote each diode, which has in serial a resister of a little value, connected in serial, and S_1, S_2, $\cdots$, S_n or S_1', S_2', $\cdots$, S_n' are the switching elements used for producing positive or negative voltage at each of points p_1, p_2, $\cdots$, p_n as shown in Fig. 1.

The pulses u_i and v_i, where i=1, 2, $\cdots$, n, are input signs applied to the switching elements S_i and S_i' respectively. Now let $(x_1, x_2, \cdots, x_n)$ and $(y_1, y_2, \cdots y_n)$ be the two

---

* Department of Electronics Engineering, College of Engineering.

bit-patterns to be compared and suppose we have logical relations

$$u_i = x_i \wedge \bar{y}_i , \qquad v_i = \bar{x}_i \wedge y_i \qquad (1)$$

such that obtain the comparison relations to a pair of bits in the two bit-patterns. This circuit can be used to decide quickly one of "greater than", "less than" and "equal to" in two bit-patterns. The most significant bit in a bit-pattern is represented by x_1. y_1 denotes the most significant bit to be compared with the reference bit x_1. And the least significant bits are x_n and y_n.

If $x_i > y_i$, u_i is true and v_i is false. Then the switching element S_i will be closed to obtain the voltage of positive polarity at the point p_i. If $x_i < y_i$, u_i is false and v_i is true. Then the switching element S_i' will be closed to obtain the voltage of negative polarity at the same point. Also, if $x_i = y_i$, both S_i and S_i' are opened and no voltage is fed into p_i. At the point P_0 this comparator can obtain the decision by sensing the three electrical states, namely positive polarity, no polarity and negative polarity.

Here we are interested in describing the original idea that has been attained to the realization of such a circuit configuration.
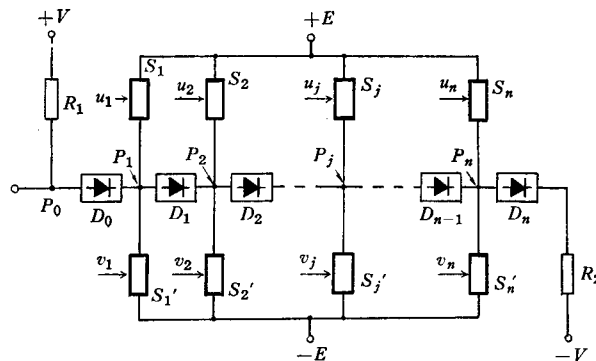

Fig. 1.   Block diagram of digital comparator.

(1)   *Theoretical approaches*

The block diagram shown in Fig. 1 can be approached by using the elementary general idea of set theory.

Definition 1:

A set K containing subsets X and Y can be classified to four subsets A, B, C and D given below:

$$\begin{aligned} A &= X \cup Y - Y \\ B &= X \cup Y - X \\ C &= X \cap Y \\ D &= K - (X \cup Y) \end{aligned} \qquad (1)$$

Then, it is clear that these four sets are subsets of a set K and also complements among these sets are all empty.

Let K be a well-ordered set representing the order of pairs to be compared with elements denoted by c_i ($i=1, 2, \cdots, n$). Then

$$(K, -\Im) = (c_1, c_2, \cdots, c_n). \tag{2}$$

Now, suppose that two bit-patterns are binary numbers, which denoted by

$$\begin{aligned} N_x &= (x_1, x_2, \cdots, x_n), & x_i \in X \\ N_y &= (y_1, y_2, \cdots, y_n), & y_i \in Y. \end{aligned} \tag{3}$$

Here x_i and y_i ($i=1, 2, \cdots, n$) are logical variables. We have the four states in combinations of a pair of bits, $(0,0)$, $(0,1)$, $(1,0)$ and $(1,1)$.

Definition 2:

By assignning an element c_i in a well-ordered set K to one of four subsets shown by eq. (1) according to the four combinations of a pair of bits (x_i, y_i), the four states representing in Def. 1 are rewritten by

$$\begin{aligned} \{c_i \,|\, x_i \bar{y}_i = 1\} &\equiv A \\ \{c_i \,|\, \bar{x}_i y_i = 1\} &\equiv B \\ \{c_i \,|\, x_i y_i = 1\} &\equiv C \\ \{c_i \,|\, \bar{x}_i \bar{y}_i = 1\} &\equiv D. \end{aligned} \tag{4}$$

The Boolean expressions $x_i \bar{y}_i = 1$ and $\bar{x}_i y_i = 1$ imply essencially relations $x_i > y_i$ and $x_i < y_i$ respectively, and both $x_i y_i = 1$ and $\bar{x}_i \bar{y}_i = 1$ take a relation $x_i = y_i$.

Theorem 3:

Statements $x_i > y_i$ and $x_i < y_i$ are equivalent to statements $c_i \in A$ and $c_i \in B$ respectively, and also a statment $x_i = y_i$ is equivalent to a statement $c_i \in C \cup D$.

Proof.

Let Q_1 be a statement $x_i > y_i$, and let R_1 be a statement $c_i \in A$. From Def. 2, it is clear that

$$Q_1 \Rightarrow R_1.$$

Next, an element c_i of the set K must belong to one of four subsets, and every intersection of subsets in K is empty.

Therefore, if R_1 then Q_1; $R_1 \Rightarrow Q_1$. Thus

$$Q_1 \Leftrightarrow R_1. \tag{a}$$

Similary, the relation between the statement $x_i < y_i$ demoted by Q_2 and $c_i \in B$ denoted by R_2 is also

$$Q_2 \Leftrightarrow R_2. \tag{b}$$

Let Q_3 be a statement $x_i = y_i$, and let R_3 be a statement $c_i \in C \cup D$. If R_3 is true, then both R_1 and R_2 are false from Def. 2, and it is also clear that both Q_1 and Q_2 are false from relations (a) and (b). Accordingly, a statment Q_3 must be true from Def. 2.

Conversely, if R_3 is false, either R_1 or R_2 is true.   In such case, Q_3 is false from (a) and (b).   Hence we will have a relation

$$Q_3 R_3 \vee \overline{Q_3}\overline{R_3} \equiv Q_3 \Leftrightarrow R_3 \,.$$

Let x_1 and y_1 be, respectively, the most significant bits in the two bit-patterns N_x and N_y, and x_n and y_n be the least significant bits in the same patterns.

A set $\{c_i\}$ $(i=1, 2, \cdots, n)$ will be a well-ordered set forming a line sequencially from higher order down to lower one, as denoted by

$$(c_1 \multimap c_2 \multimap c_3 \multimap \cdots \multimap c_n) \,.$$

Definition 4:

Let a set P be a direct sum of A and B;

$$P = A + B \,.$$

Set P is also a well-ordered set and contains only such elements that obtain the decision for comparisons of each ordered pair.

Theorem 5:

The first element of the set P, denoted by *min* P, is either *min* A or *min* B.

Proof:

Assume P is a non-empty set.   Thus, there exists a element *min* P, denoted by c_m. If $c_m \in A$, then $c_m = min$ A, and if $c_m \in B$, then $c_m = min$ B.

Next, suppose subsets A, B are both non-empty sets. there exist *min* A and *min* B, denoted respectively by c_k and c_l, in the set P.   And these elements must mutually take either the order $c_k \multimap c_l$ or $c_l \multimap c_k$.   Thus c_m will be equally either c_k or c_l from Def. 4.

Theorem 6:

(1) $N_x = N_y$ iff $c_i \in C \cup D$, $(i=1, 2, \cdots, n)$
(2) $N_x > N_y$ iff $c_m \in A$,
(3) $N_x < N_y$ iff $c_m \in B$.

Proof for (1):

From Theorem 3, it is clear that $x_i = y_i$ iff $c_i \in C \cup D$.   If $N_x = N_y$, relations for all pairs will be $x_i = y_i$.   Theorem 3 must be organized for all indexes i.

Proof for (2) and (3):

If $N_x > N_y$ or $N_x < N_y$, there exists at least one of n elements in the set P and one of them must be a element c_m of the highest order in elements that belong to the set P.

From Theorem 3, it is clear that

$$x_m < y_m \quad \text{iff} \quad c_m \in A$$

and

$$x_m < y_m \quad \text{iff} \quad c_m \in B \,.$$

Hence, $x_m > y_m$ and $x_m < y_m$ are respectively equivalent to $N_x > N_y$ and $N_x < N_y$, for there exist no elements c_i such that $c_i \bar{\bar{3}} c_m$ in the set P.

Hence, with associations between the general consideration above and the actions of the comparator as shown in Fig. 1, it follows that

(1) The elements $c_1, c_2, \cdots, c_n$ in a well-ordered set K are regarded as on-off states of each pair of switches.

(2) Let u_i be the output of implication logic $x_i \bar{y}_i$, and v_i be the output of another implication logic $\bar{x}_i y_i$. If $u_i = 1$, then the switch S_i is on and S_i' is off. Such a state of the switch will be equivalent to the statement $c_i \in A$. In the case of $v_i = 1$, the state of the switches S_i, S_i' will be equivalent to $c_i \in B$. And also if $u_i = v_i = 0$, then both switches are off, and this state will be equivalent to $c_i \in C \cup D$.

(3) If $c_i \in A$, the positive voltage would be fed into a point p_i on a line of serial diodes through S_i and if $c_i \in B$, the negative voltage would be fed into p_i.

(4) If $u_k = 1$ and $v_l = 1$, where k, l are indexes that denoted in Theorem 5, then output voltage at a point p_0 indicates positive or negative polarity according to $k < l$ or $l < k$. Such actions of serial diodes would be explained by two statements in Theorem 6.

(2) *Boolean expressions*

The decision of the comparison for the two bit-patterns will be directly induced by Boolean expressions.

We use again relations shown in eq. (1) for two bit-patterns $(x_1, x_2, \cdots, x_n)$ and $(y_1 y_2 \cdots, y_n)$. Imagine a circuit in which all switches between a pair of $j+1$ th, (S_{j+1}, S_{j+1}'), and a final pair, (S_n, S_n'), are removed from a comparator shown in Fig. 1. Now, let F_j^+ be a logical function such that takes 'one' if such comparator indicates positive polarity at a point p_0 in it.

Then for all combinatins among logical variables $u_1, u_2, \cdots, u_j, v_1, v_2, \cdots, v_j$, suppose relations as follows;

$$F_j^+ = f(u_1, u_2, \cdots, u_j, v_1, v_2, \cdots, v_j) \tag{5}$$

and at the point p_j,
$$k_j = u_j \bar{v}_j . \tag{6}$$

Next, suppose the circuit in which a pair of $j+1$ th is added to the above circuit, then the relation (6) will be replaced by

$$k_j' = \bar{v}_j (u_j \lor k_{j+1}) \tag{7}$$

Applying eq. (6) to eq. (7) gives

$$k_j' = \bar{v}_j u_j' , \tag{8}$$

where
$$u_j' = u_j \lor u_{j+1} \bar{v}_{j+1} .$$

Then, containing variable u_{j+1} and v_{j+1} in eq. (5) gives

$$F_{j+1}^+ = f(u_1, u_2, \cdots, u_{j+1}, v_1, v_2, \cdots, v_{j+1}) \tag{9}$$

and using from eq. (5) to eq. (9) gives

$$F^+_{j+1} = f(u_1,\, u_2,\, \cdots,\, u_{j-1},\, u'_j,\, v_1,\, v_2,\, \cdots,\, v_j)\,. \qquad (10)$$

From eq. (5) and (10), it will be found that the logical function F^+_{j+1} can be given by the relation with u_j and u'_j ($1 \leq j \leq n-1$), transposed in eq. (5).

If $j=1$, then eq. (5) will be given by

$$F^+_1 = u_1 \bar{v}_1\,. \qquad (11)$$

Thus, applying eq. (10) for all variables will give

$$F^+_n = \bar{v}_1\{u_1 \vee \bar{v}_2\{u_2 \vee \cdots \bar{v}_i\{u_i \vee \bar{v}_{i+1}\{u_{i+1} \vee \cdots \vee \bar{v}_{n-1}\{u_{n-1} \vee \bar{v}_n u_n\}\}\cdots\}_{n-1}\,. \qquad (12)$$

Also, applying eq. (1) to eq. (12) gives

$$F^+_n = x_1 \bar{y}_1 \vee (x_1 \vee \bar{y}_1)\{x_2 \bar{y}_2 \vee (x_2 \vee \bar{y}_2)\{\cdots\cdots$$
$$\cdots\cdots (x_{n-2} \vee \bar{y}_{n-2})\{x_{n-1}\bar{y}_{n-1} \vee (x_{n-1} \vee \bar{y}_{n-1}) x_n \bar{y}_n\}\}\cdots\}_{n-1}\,. \qquad (13)$$

We may be similarly analyzed the logical relation F^-_n such that results the negative voltage to the output termination p_0. Hence F^-_n will be simply given by the relation with x_i and y_i, transposed in eq. (13), that is

$$F^-_n = \bar{x}_1 y_1 \vee (\bar{x}_1 \vee y_1)\{\bar{x}_2 y_2 \vee (\bar{x}_2 \vee y_2\{\cdots\cdots$$
$$\cdots\cdots (\bar{x}_{n-2} \vee y_{n-2})\{\bar{x}_{n-2} y_{n-1} \vee (\bar{x}_{n-1} \vee y_{n-2})\bar{x}_n y_n\}\cdots\}_{n-1}\,. \qquad (14)$$

The equation (13) implies that $N_x > N_y$ if $F^+_n = 1$ and $N_x \leq N_y$ if $F^+_n = 0$. The equation (14) implies that $N_x < N_y$ if $F^-_n = 1$ and $N_x \geq N_y$ if $F^-_n = 0$. If the output shows zero, N_x is equal to N_y, and then $F^+_n = F^-_n = 0$. As an example, the relation (13) will be denoted by logic as shown in Fig. 2. This logic is well known as the circuit[2] which is used to decide either $N_x > N_y$ or $N_x \leq N_y$, but can not obtain a decision among $N_x > N_y$, $N_x < N_y$ and $N_x = N_y$.
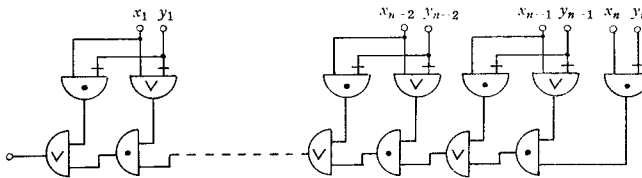

Fig. 2.   Logic for $N_x > N_y$.

3.   Circuits and experiments

Fig. 3 shows a digital comparator[3] realized to perform the tests of comparative behaviors. The two lattice circuits consisted of R and C are voltage sources; one is the positive source and another is the negative. Resistors, denoted by R, dividing equally voltage $E^+_1 - E^+_2$ or $E^-_1 - E^-_2$ with $n+1$ are used to compensate the potential difference of each diode. The resisters, denoted by r, are inserted for current limiting. The comparator shown in Fig. 3 has the comparative function for patterns of 6 bits.
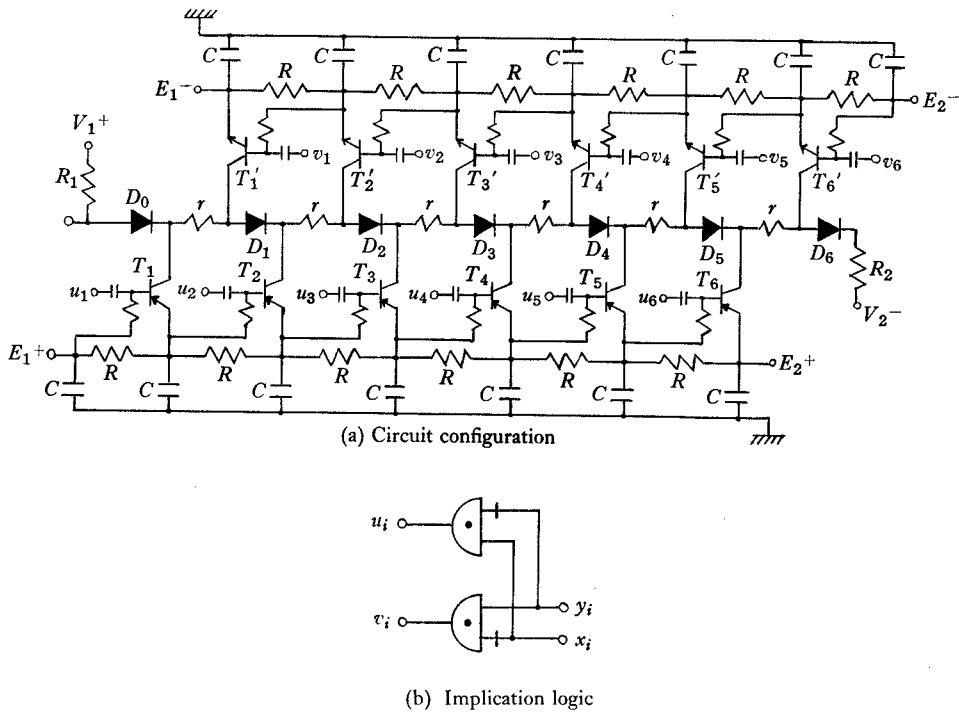
(a) Circuit configuration

(b) Implication logic

Fig. 3. Digital comparator circuit.

Pulses $u_1, u_2, \cdots, u_n$, provided as inputs to each of switching transistors $T_1, T_2, \cdots, T_n$, have to take negative polarity, while $v_1, v_2, \cdots, v_n$, provided as inputs to each of $T_1', T_2', \cdots, T_n'$, have to take the positive. And these pulses are generated by implication logics as shown together in Fig. 3.

For example, let

$$N_x = (011101)_2 \qquad N_y = (010110)_2$$

be two binary numbers to be compared. Then pulses u_3, u_6 and v_5 are provided to close the trasistors corresponding. Accordingly, the circuit connected between positive and negative sources is only T_3 D_3 D_4 T_5' and then the polarity at the point p_3 shows positive. Accordingly, the output of the comparator takes the positive pulse and obtains the decision such that $N_x > N_y$.

This comparator, in reality, makes use of a shaping circuit, connected with the point p_0, which produces separately positive and negative pulses.

A comparator, which can perform the comparative operations for more long length of bit-patterns, will be realized by a configuration shown in Fig. 4. The circuit of such system as shown in Fig. 3 unfits for the comparison of the two bit-patterns such as run into scroes of bits, because of voltage drops of each serial diode and long carry propagation time. We found the system shown in Fig. 4 by dividing bit-patterns to be compared into some groups, each of which consists of several bits. These groups, denoted by C_1, C_2,

$\cdots$, C_n, have the comparative function as well as shown in Fig. 3 and obtain the comparative decisions nealy at once. The final comparative decision will be obtained by a group C_0, which is equivalent to groups above.
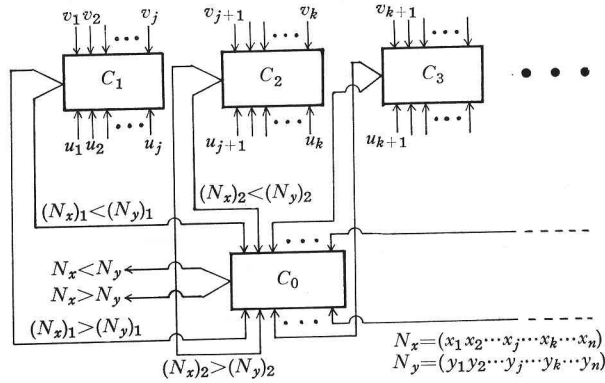

Fig. 4.   Comparator system for the long length bit-pattern.

Experiments were done to ascertain the operations of the comparison with the circuit shown in Fig. 3.   Photo. 1 shows the iterative waveforms of a switching pulse (a) and an output pulse (b) generated by the shaping circuit.   The result shown in (b) is a waveform which obtains the decision between two binary numbers $(001010)_2$ and $(000101)_2$ as an example.   This comparator operated accuratly as well for many other examples.
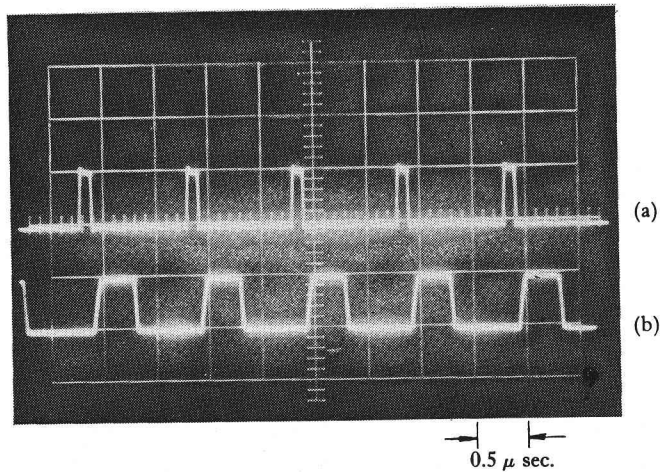

0.5 μ sec.

Photo. 1.   The iterative waveform of a switching pulse v_4 of $1V$
(a) and an output pulse of $5V$ (b).

4.   Conclusions

A new digital comparator was realized by applying the general idea of set theory.   As mentioned above, this comparator can obtain a decision among $N_y > N_x$, $N_x < N_y$ and

$N_x = N_y$, by detecting three electrical states; positive polarity, negative polarity and no polarity, and be designed with simple circuit configurations. Further this circuit will be able to perform more quickly operation by employing high speed switching components in it, and also will be applied to nearly all data-processing systems.

References

1) R.A. Hedin, Electronic Design, **13,** Oct. 11 (1965).
2) Computer Handbook, Information Processing Society of Japan Press, p. 2–98 (1966).
3) H. Kosako, K. Oshima and Y. Kojima, Lecture in Annal Joint Meeting of I.E.C.E. of Japan (1966).